

Analog:

Analog quantities vary continuously, and analog systems represent the analog information using electrical signals that vary smoothly and continuously over a range.

Digital:

Digital quantities vary in discrete levels. In most cases, the discrete levels are just two values ON and OFF. Digital systems carry information using combinations of ON/OFF electrical signals that are usually in the form of codes that represent the information.

both data about the physical world and control signals sent to interact with the physical world are typically "analog" or continuously varying quantities.

when data is in binary form, the 0's and 1's may be of several forms such as the TTL form where the logic zero may be a value up to 0.8 volts and the 1 may be a voltage from 2 to 5 volts.

the data can be converted to clean digital form using gates which are designed to be on or off depending on the value of the incoming signal

Data in clean binary digital form can be converted to an analog form by using a summing amplifier.

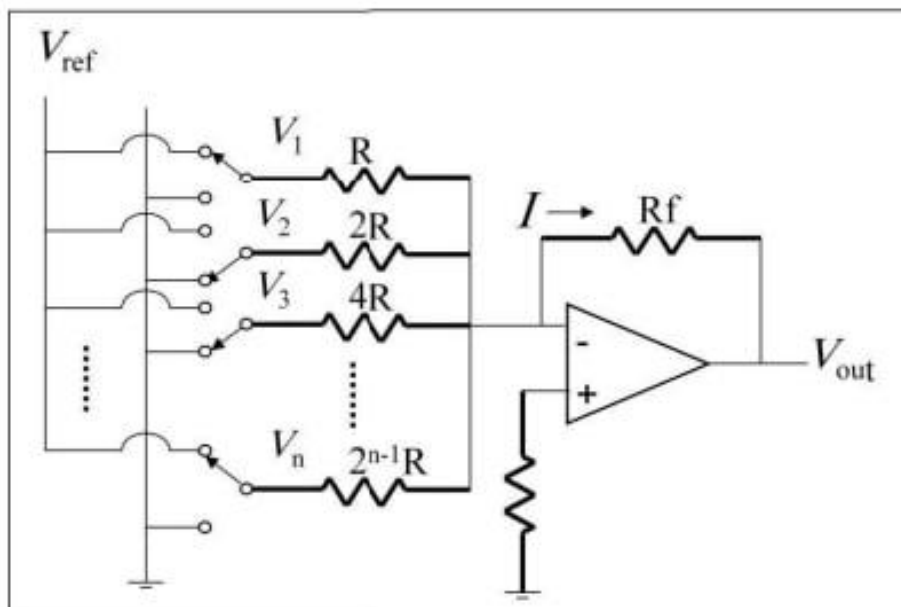
two basic approaches to convert :

1-Weighted summing amplifier

2-R-2R Network Approach

1-Weighted summing amplifier

the weighted sum DAC is not satisfactory for a large number of bits because it requires too much precision in the summing resistors this problem is overcome in the R-2R network DAC



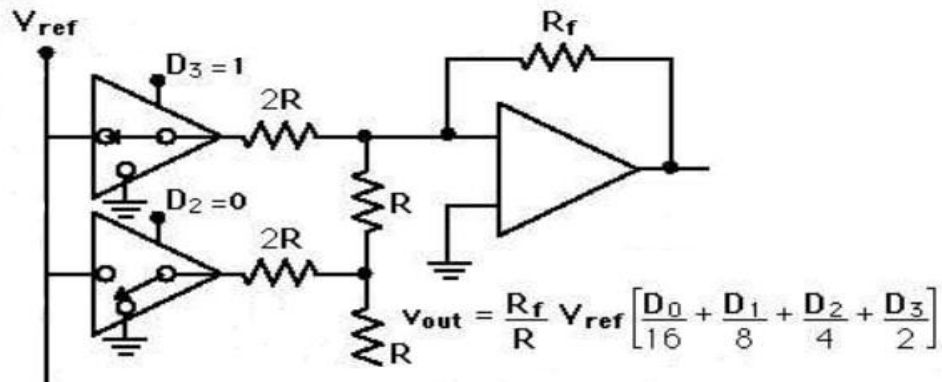
For example, a 4-Bit converter yields

$$V_{out} = -V_{ref} \left(b_3 \frac{1}{2} + b_2 \frac{1}{4} + b_1 \frac{1}{8} + b_0 \frac{1}{16} \right)$$

Where b_3 corresponds to Bit-3, b_2 to Bit-2, etc.

2-R-2R Network Approach

network of resistors, called a ladder network. A ladder network accepts inputs of binary values at, typically, 0 V or V_{ref} and provides an output voltage proportional to the binary input value.



The digital inputs could be TTL voltages which close the switches on a logical 1 and leave it grounded for a logical 0
can use this approaches to any number of bits by use this equation:

$$V_{\text{out}} = -V_{\text{ref}} \sum_{i=1}^n b_{n-i} \frac{1}{2^i}$$

advantages :

- 1-only two resistor values (R and 2R)
- 2-does not require high precision resistors

disadvantages :

- 1- lower conversion speed than binary weighted DAC

Resolution :

smallest analog increment corresponding to 1 LSB change

An N-bit resolution can resolve 2^N distinct analog levels

$$\text{Resolution} = V_{\text{LSB}} = \frac{V_{\text{ref}}}{2^N}$$

Analog to Digital Conversion [ADC]

The basic principle of operation is to use the comparator principle to determine whether or not to turn on a particular bit of the binary number output.

It is typical for an ADC to use a digital-to-analog converter (DAC) to determine one of the inputs to the comparator.

Conversion process:

Sampling

Quantification

Coding

Conversion process: sampling

Digital system works with discrete states

the signal is only defined at determined times

the sampling times are proportional to the sampling period (T_s)

Conversion process: Quantification

the signal can only take determined values belonging to a range of conversion

based on number of bit combinations that the converter can output

number of possible states: $N=2^n$ where n is number of bits

Resolution: $Q = \Delta V_r / N$

ADC Various Approaches:

Digital-Ramp ADC

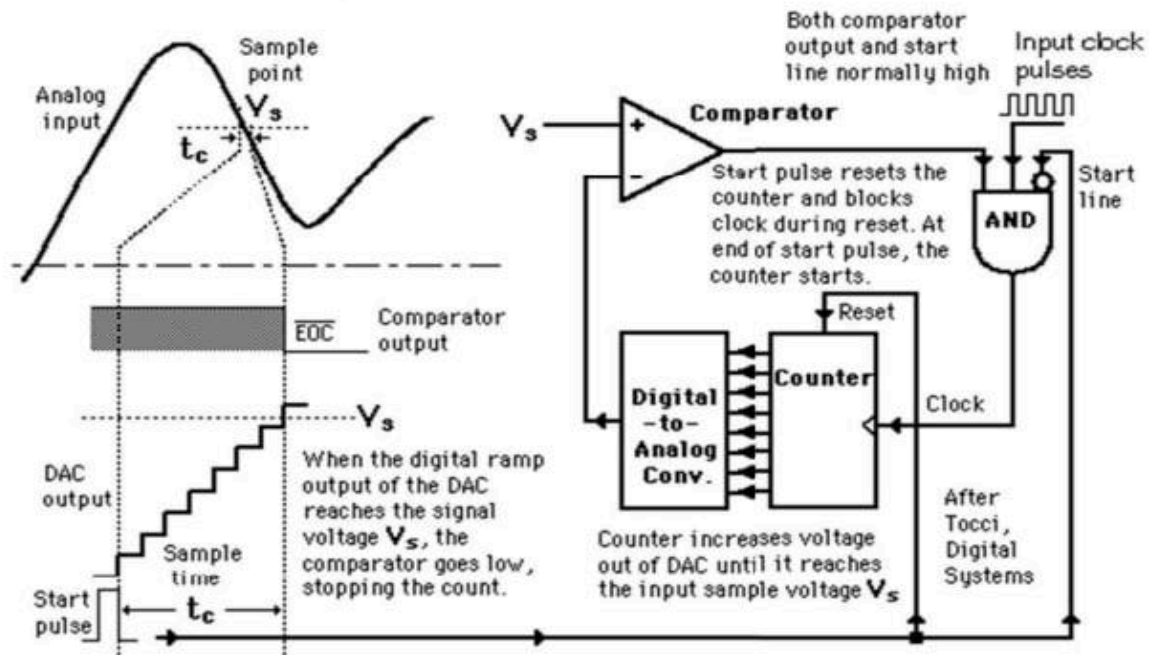
Successive Approximation ADC

Flash ADC

Digital-Ramp ADC

conversion from analog to digital form inherently involves comparator action where the value of the analog voltage at some point in time is compared with some standard.

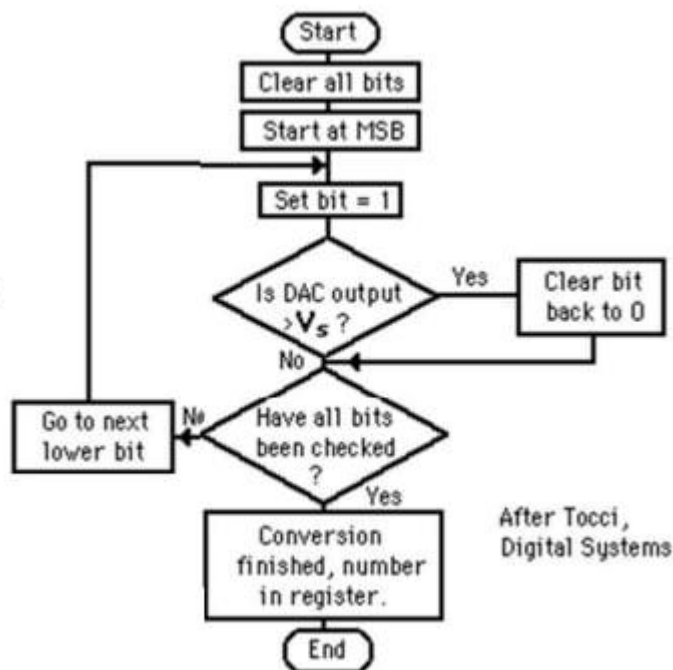
A Common way to do that is to apply the analog voltage to one terminal of a comparator and trigger a binary counter which drives a DAC.



Successive Approximation ADC

Much faster than the digital ramp ADC because it uses digital logic to converge on the value closest to the input voltage

A comparator and a DAC are used in the process



Advantages:

capable of high speed

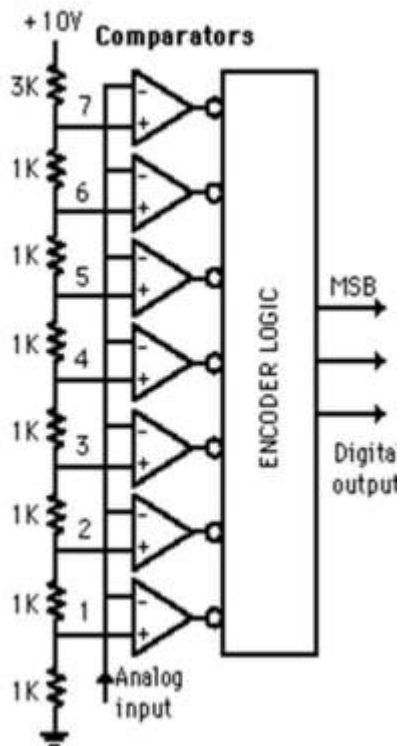
medium accuracy compared to other ADC types

Good tradeoff between speed and cost

Disadvantages:

Higher resolution successive approximation ADCs will be slower
speed limited ~5Msps

Flash ADC



it is the fastest type of ADC available, but requires a comparator for each value of output.

such ADCs are available in IC form up to 8-bit and 10-bit flash ADCs (1023 comparators) are planned.

The encoder logic executes a truth table to convert the ladder of input to the binary number output.

The resistor net and comparators provide an input to the combination logic circuit, so the conversion time is just the propagation delay through the network - it is not limited by the clock rate or some convergence sequence.

Advantages:

very fast

Disadvantages:

needs many parts (255 comparators for 8-bit ADC)

lower resolution

Expensive

large power consumption

ADC080x Features

compatible with 8080 up derivatives - no interfacing logic needed -

access time - 135ns

easy interface to all microprocessors, or operates "stand alone"

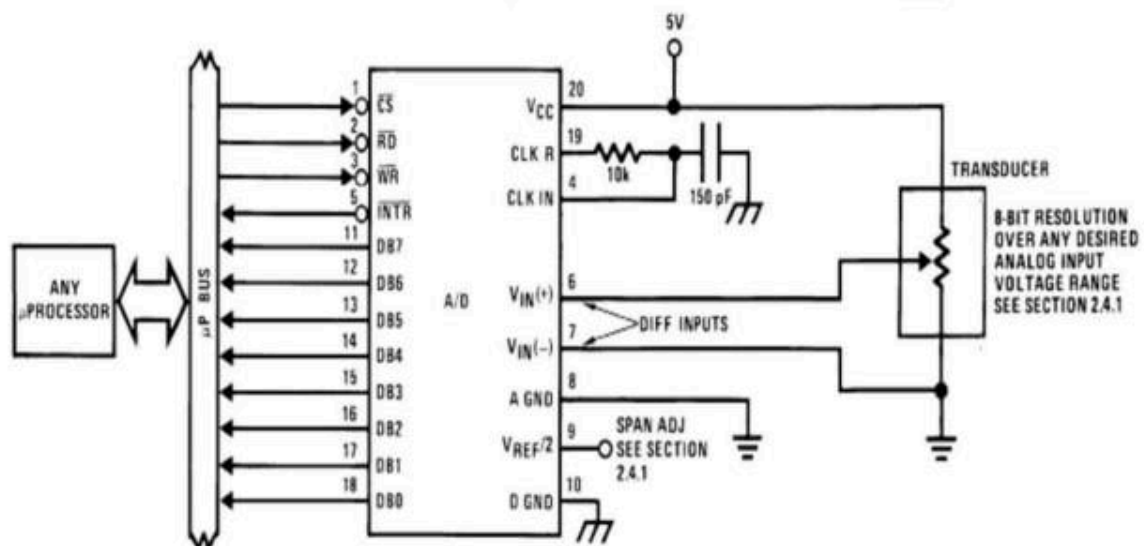
differential analog voltage inputs

logic inputs and outputs meet both MOS and TTL voltage level specifications

0V to 5V analog input voltage range with single 5V supply

No zero adjust required

ADC080x, interfacing



DS005671-1

IN dest, source

OUT dest, source

MOV DX, port

BACK MOV DX, 300H

JMP BACK

There are two primary methods for microprocessors to interface with I/O devices: isolated I/O and memory-mapped I/O.

Isolated I/O (port-mapped I/O) utilizes specific IN, INS, OUT, and OUTS instructions to transfer data between the CPU (accumulator or memory) and I/O devices. It features a separate I/O address space, distinct from memory, allowing the full memory space to be used for memory. However, it requires dedicated I/O instructions and separate control signals (IOR and IOW). PCs primarily use isolated I/O for controlling peripherals via I/O ports (8-bit for onboard devices, 16-bit for others).

Memory-Mapped I/O, in contrast, treats I/O devices as memory locations. It uses any memory transfer instruction to communicate with I/O devices. The key advantage is the flexibility of using any memory instruction. The main disadvantage is that a portion of the memory address space is reserved for I/O, reducing the memory available for applications.

Additionally, the

IOR and IOW

signals are not used, potentially simplifying decoding circuitry.

The PC reserves the I/O port address range 0000H to 03FFH for core system functions and the ISA bus.

The I/O port range 0400H to FFFFH is generally available for user applications, mainboard functions, and the PCI bus.

Specifically, the 80287 math coprocessor uses I/O addresses 00F8H to 00FFH for communication. Consequently, Intel reserves the range 00F0H to 00FFH. Later processors like the 80386 to Core2 use a higher address range (800000F8H to 800000FFH) for their coprocessor communication.

I/O ports in the lower range (0000H to 00FFH) are accessed using fixed port I/O instructions, while ports in the upper range (above 00FFH) are accessed using variable I/O port instructions.

handshaking : Many I/O devices accept or release information at a much slower rate than the microprocessor. another method of I/O control, called handshaking or polling synchronizes the I/O device with the microprocessor. An example of a device that requires handshaking is a parallel printer that prints a few hundred character per second (CPS). it is obvious that the microprocessor can send more than a few hundred CPS to the printer, so a way to slow the microprocessor down to match speeds with printer must be developed.

large current loads such as motors or large relays require a Darlington pair in place of the transistor driver