

((analog diagram
circuit diagram))

①

Q Determine the analog diagram and circuit diagram to implement the

$$V_0 = -0.25 V_1 + 6.34 V_2 + 3.3$$

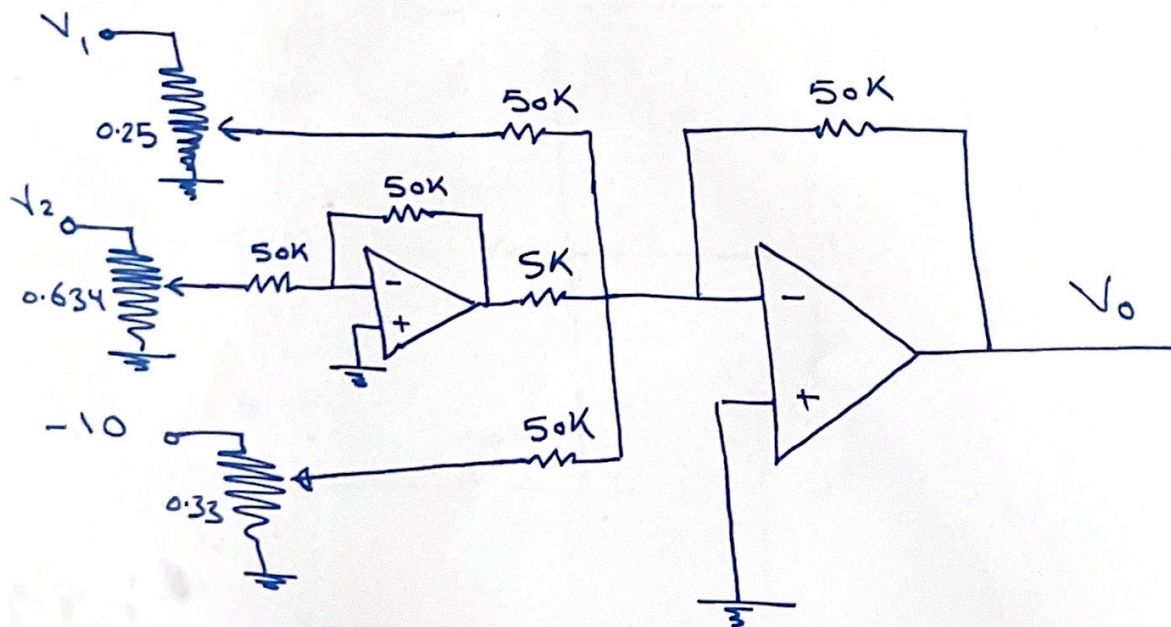
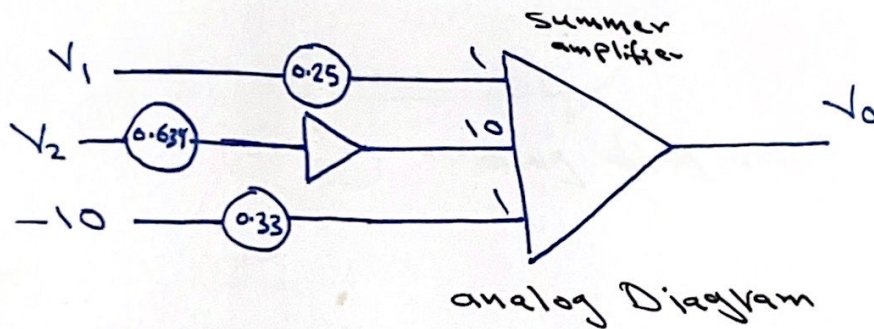
ans

$$0.25 \rightarrow 0.25 V_1$$

$$6.34 \rightarrow 0.634 \times 10 V_2$$

$$3.3 \rightarrow 0.33 \times 10$$

درجہ اولیٰ، ثانی، تیسری



Ex

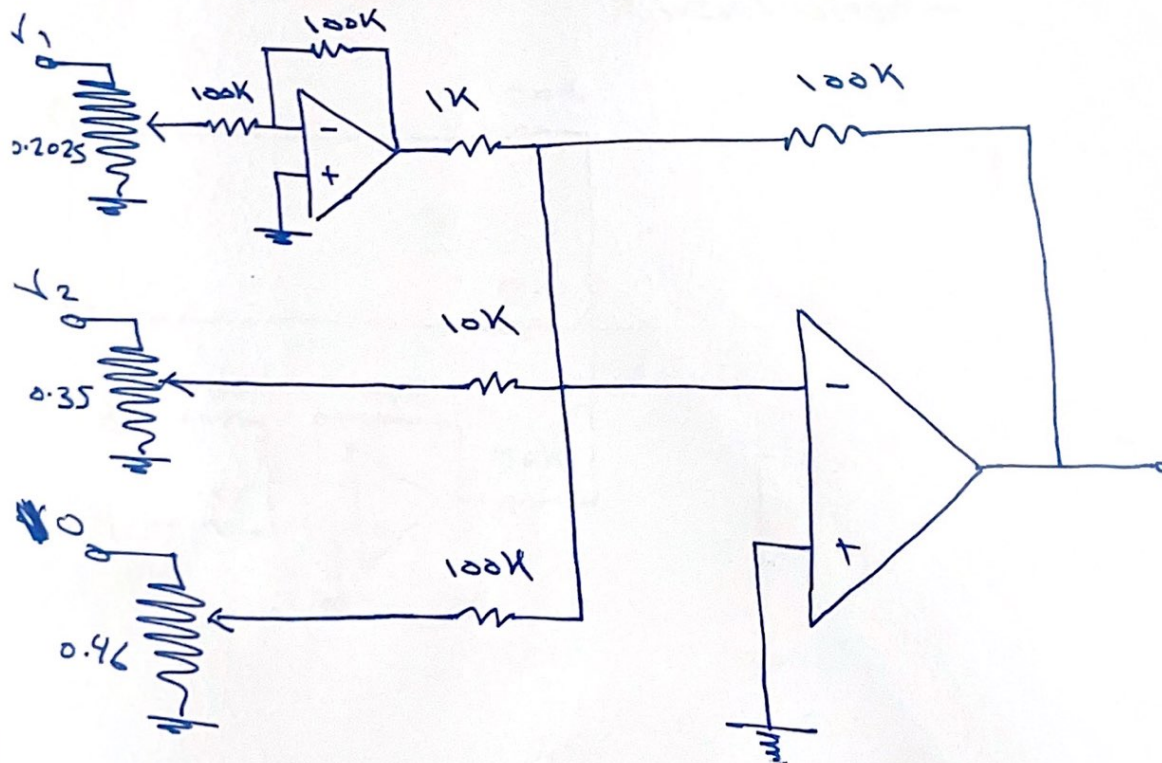
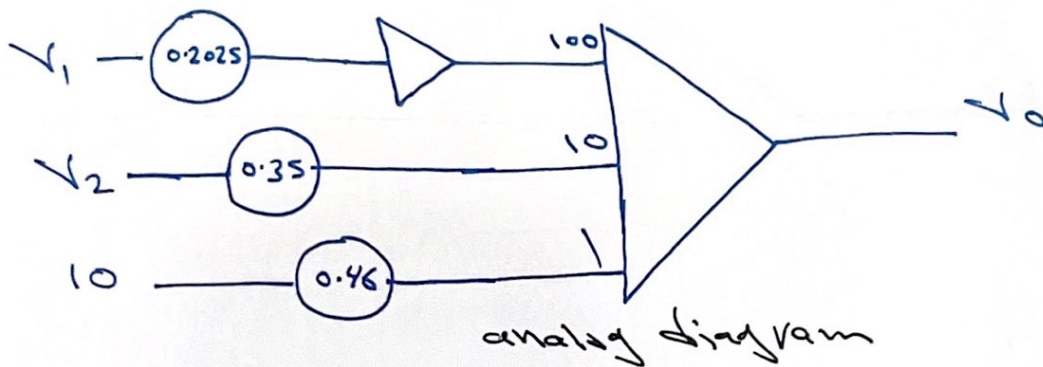
$$V_0 = 20.25V_1 - 3.5V_2 - 4.6$$

ans

$$20.25 \rightarrow 0.2025 \times 100 \quad V_1$$

$$3.5 \rightarrow 0.35 \times 10 \quad V_2$$

$$4.6 \rightarrow 0.46 \times 10$$

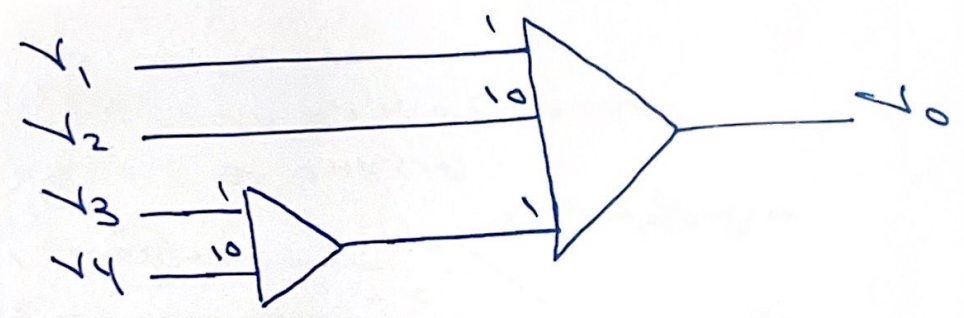


Q5 Determine the analog diagram
and circuit diagram to implement
the equation

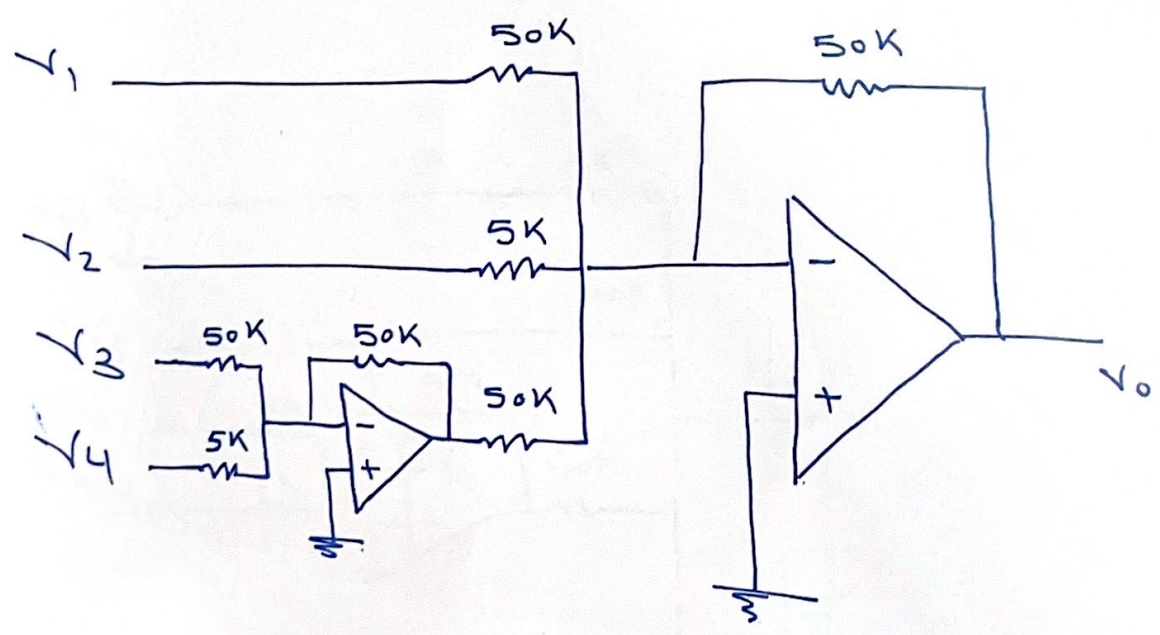
$$V_o = -V_1 - 10V_2 + V_3 + 10V_4$$

Ans

analog computer



circuit diagram



Ex Determine the analog diagram and circuit diagram to implement the equation.

$$V_o = -3.3V_1 + 10V_2 - 5V_3 + 6.25V_4 + 4.5$$

ans

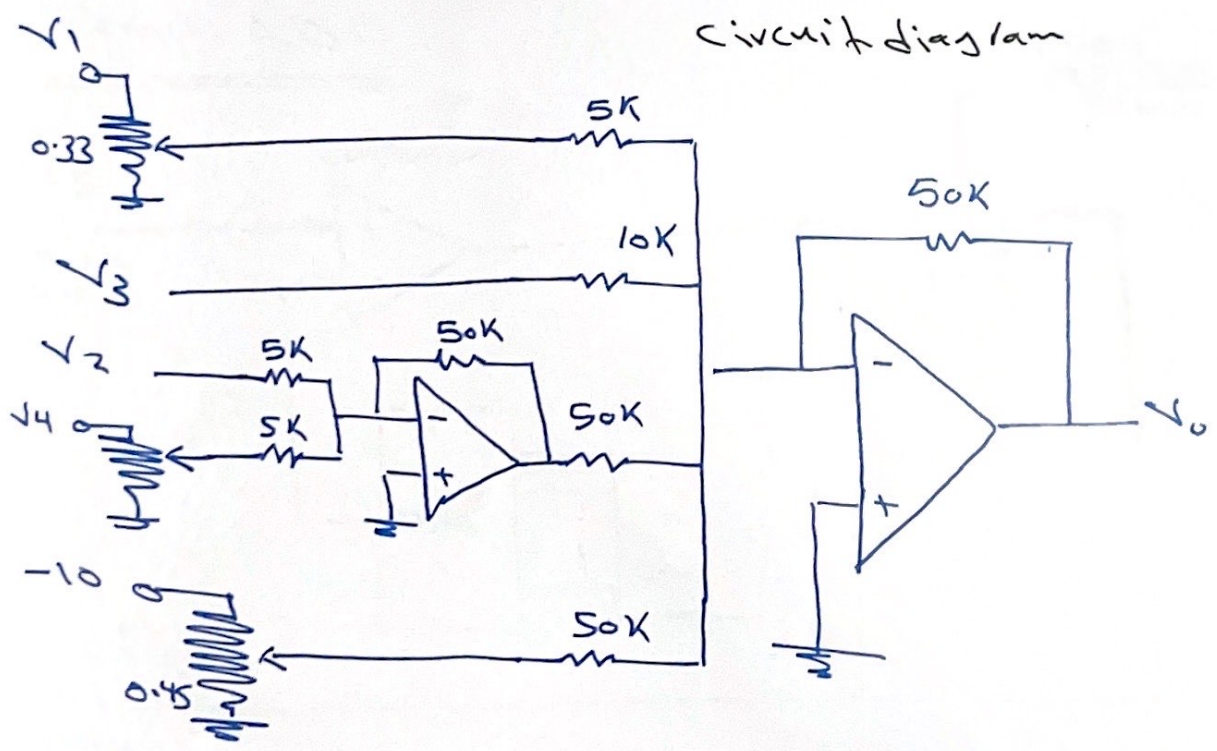
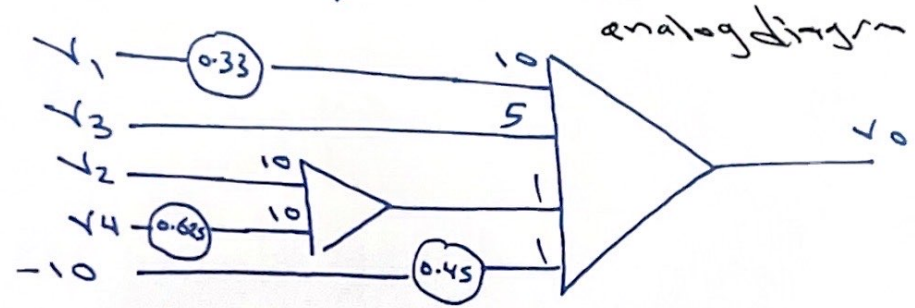
$$-3.3V_1 \Rightarrow -0.33 \times 10V_1$$

$$-5V_3$$

$$+10V_2$$

$$+6.25V_4 \Rightarrow +0.625 \times 10V_4$$

$$4.5 \Rightarrow 0.45 \times 10$$



ADC

5

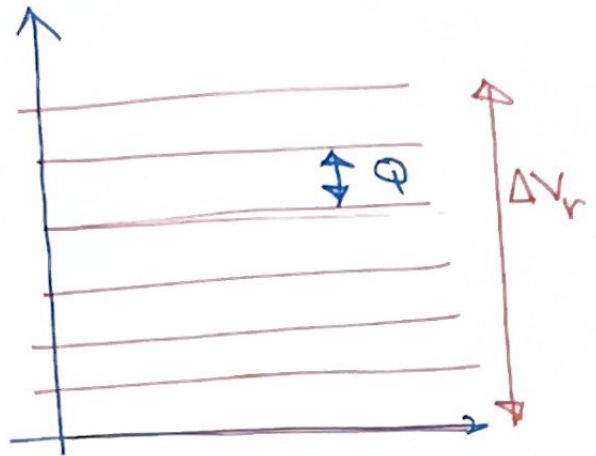
Analog to Digital converter

ΔV_r : range of voltage

Q : resolution

$$\text{no. of level} = 2^N$$

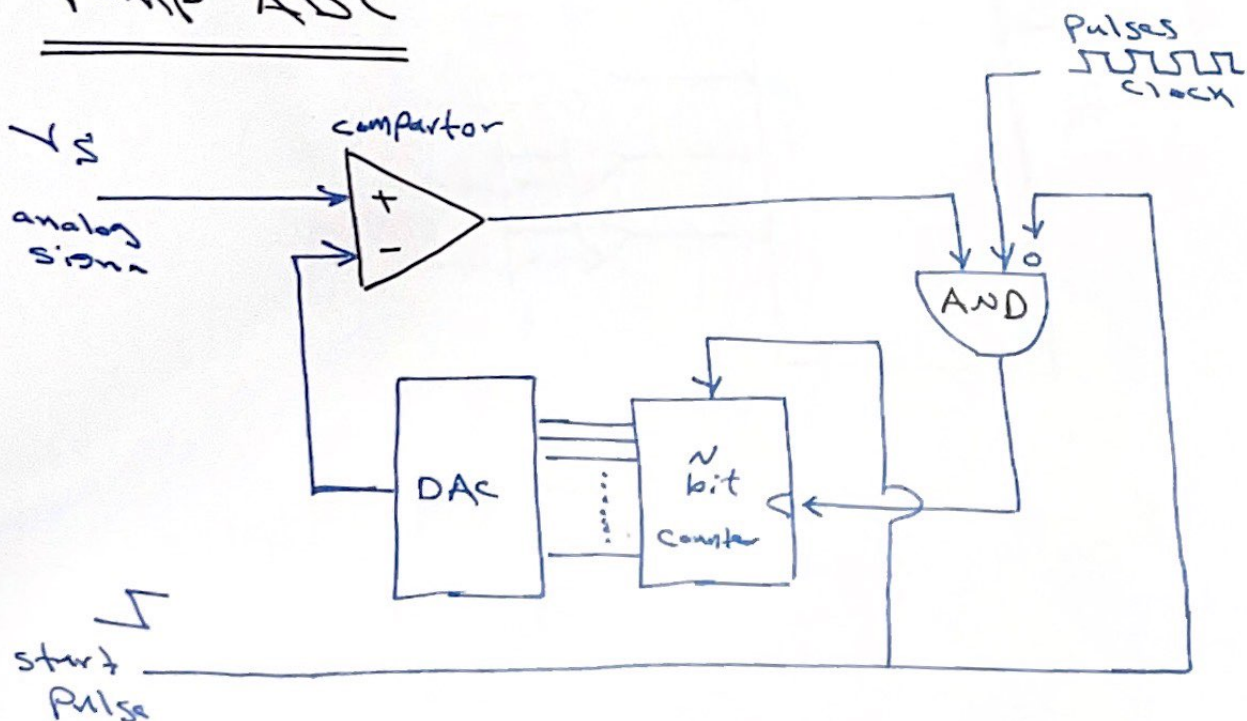
N = no. of bit



$$\text{resolution} = Q = \frac{\Delta V_r}{2^N}$$

note $\Delta V_r = V_{ref}$

Ramp ADC



Flash ADC

⑥

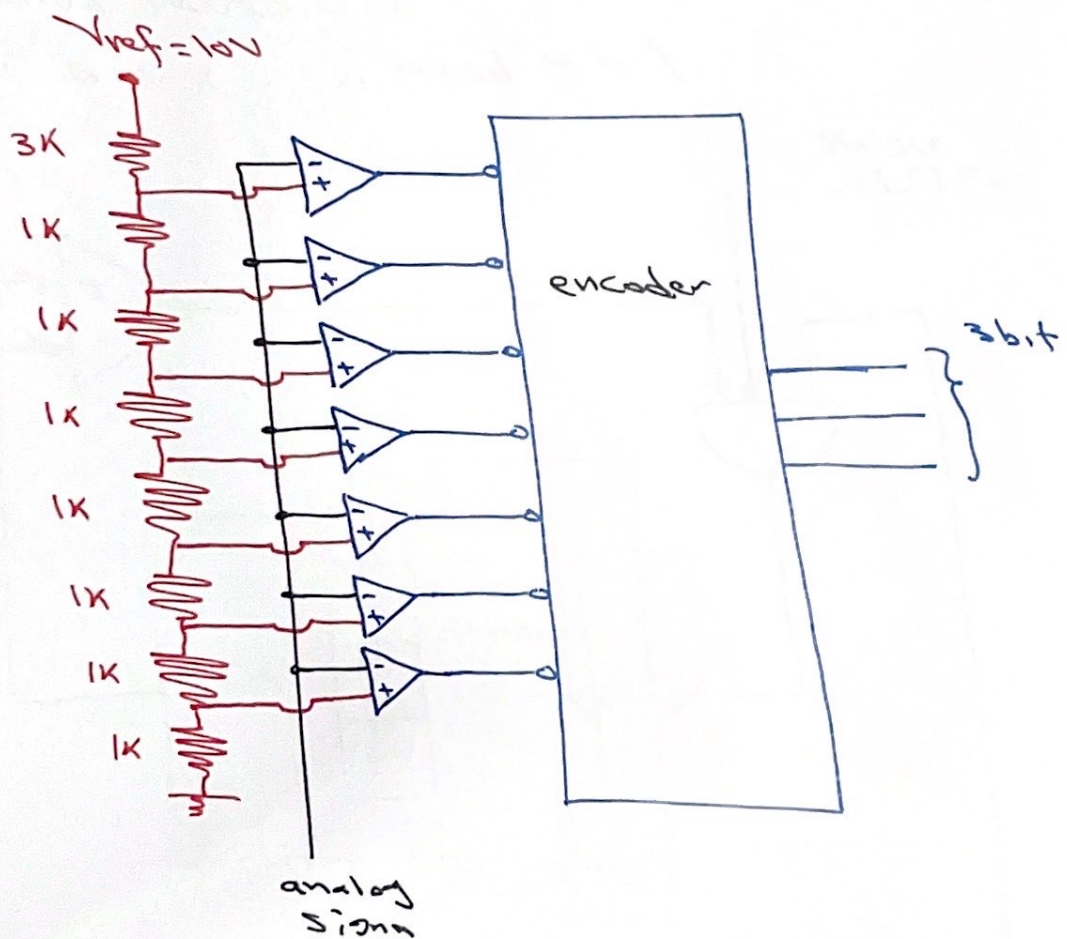
$$\text{no. of comparators} = 2^N - 1$$

if 8 level

$$\therefore 8 = 2^3 = 2^N$$

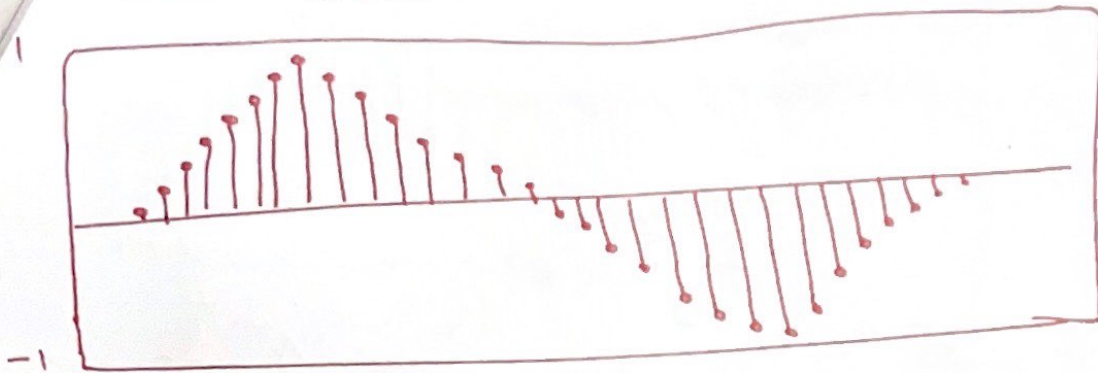
$$\therefore N = 3 \text{ bit}$$

$$\text{no. of comparators} = 2^3 - 1 = 7$$



Design digital ramp ADC for following

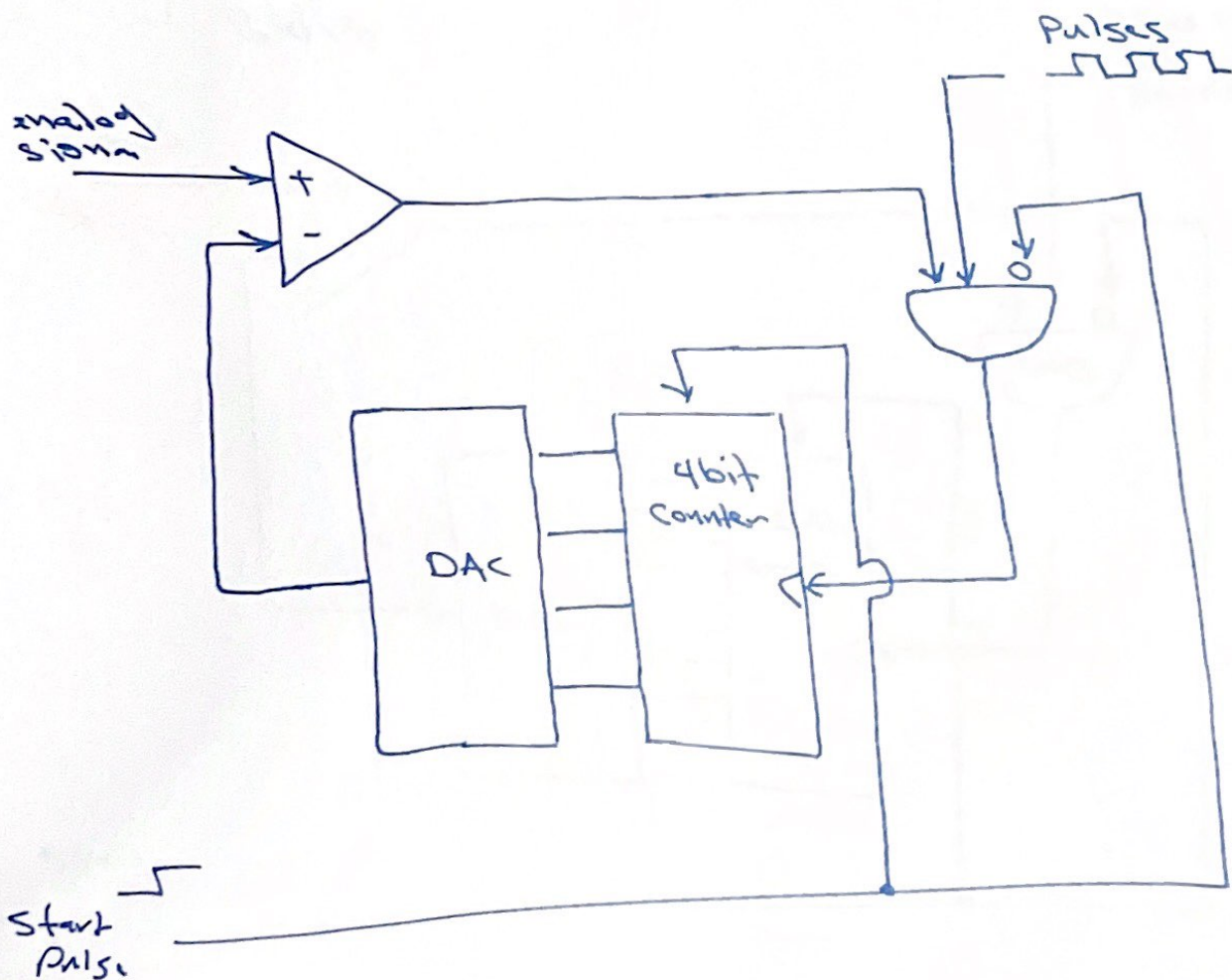
(7)



ans from graph

no. of level = 16

$\therefore 16 = 2^4 \therefore$ need 4 bit



Q4 Design digital ramp ADC if the voltage (5V) and the resolution (19.5mV) and filter frequency (200Hz)

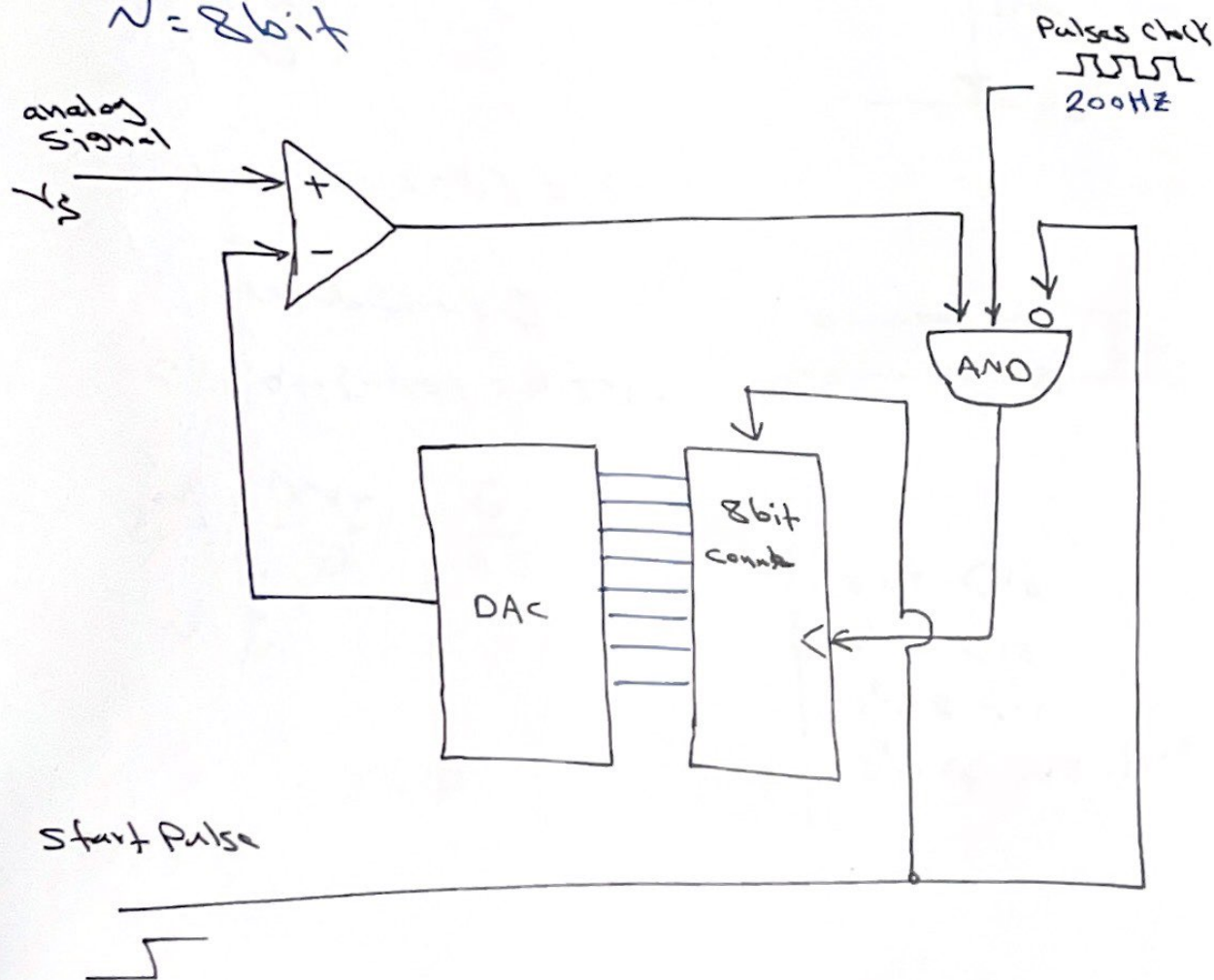
ans

$$\text{resolution} = Q = \frac{\Delta V_r}{2^N}$$

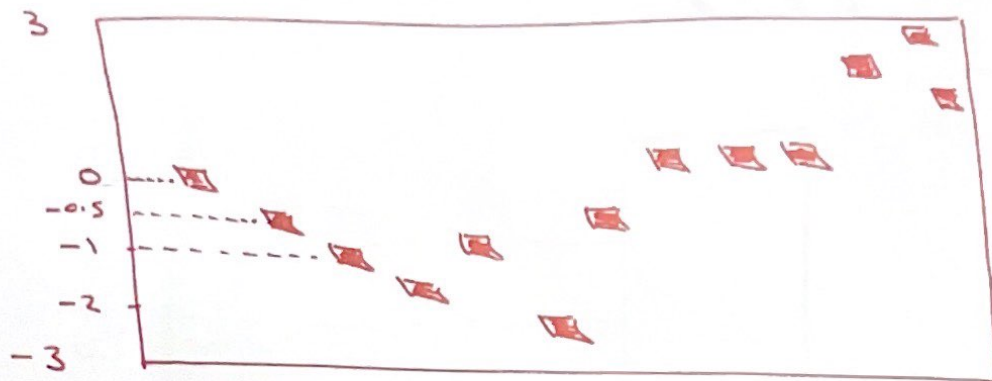
$$2^N = \frac{\Delta V_r}{Q} = \frac{5}{19.5 \times 10^{-3}} = \frac{5}{0.0195} = 256$$

$$2^N = 256 = 2^8$$

$$N = 8 \text{ bit}$$

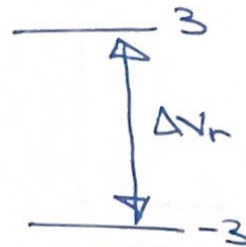


Q Design a flash ADC for the following signal



ans $Q = \frac{\Delta V_r}{2^N}$

$2^N = \frac{\Delta V_r}{Q}$



$\Delta V_r = 3 - (-3) = 6$

$\therefore$ resolution = Q

$Q = 0 - (-0.5) = 0.5V$



$2^N = \frac{\Delta V_r}{Q} = \frac{6}{0.5}$

$2^N = 12$

$\therefore 2^4 = 16 > 12$

$\therefore N = 4 \text{ bit}$

$2^1 = 2 < 12$

$2^2 = 4 < 12$

$2^3 = 8 < 12$

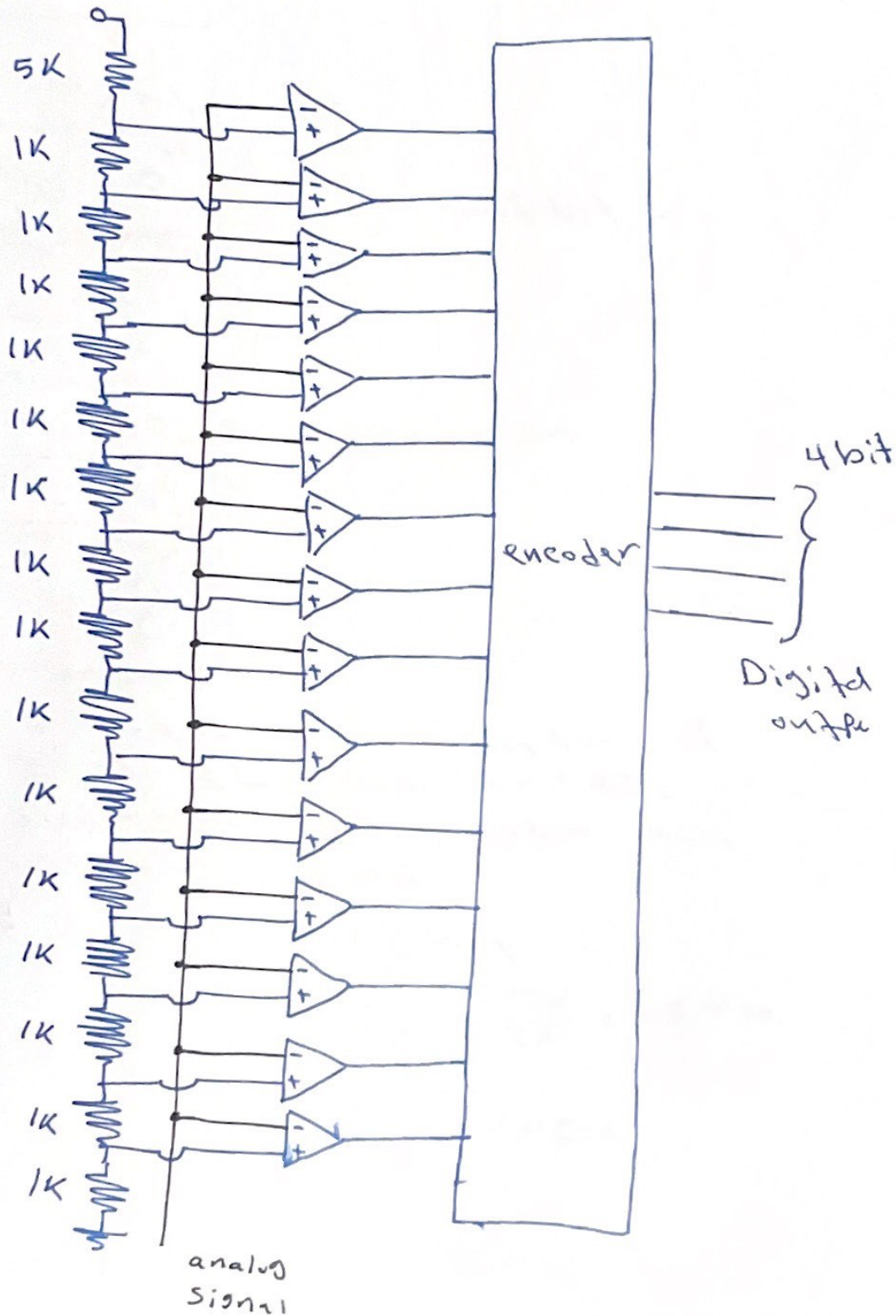
$2^4 = 16 > 12 \checkmark$

∴ Flash ADC

(10)

$$\text{no. of comparators} = 2^4 - 1 = 16 - 1 = 15$$

$$V_{ref} = 10V$$



conversion time T_c

(11)

$$T_c = \frac{n_c}{f}$$

→ Digital ramp

$$n_c = 2^n$$

n : no. of bit.

$$T_c = \frac{2^n}{f}$$

→ Successive approximation

$$n_c = n$$

$$T_c = \frac{n}{f}$$

Q. Find maximum conversion time of
① a 8 bit Stair case ramp ADC
② a successive approximation ADC
if clock rate is 2 MHz

Ans $f = 2 \text{ MHz}$ $n = 8 \text{ bit}$

$$\text{① } T_c = \frac{n_c}{f} = \frac{2^n}{f} = \frac{2^8}{2M} = \frac{256}{2M} = 128 \mu\text{sec}$$

$$\text{② } T_c = \frac{n_c}{f} = \frac{n}{f} = \frac{8}{2M} = 4 \mu\text{sec}$$

2015

(12)

Q2 - Calculate the maximum conversion time of Successive approach ADC if the clock rate 20MHz, and number of bit 8 bits

ans

$$T_c = \frac{n_c}{f}$$

∴ Successive approach

$$\therefore n_c = n = 8$$

$$T_c = \frac{8}{20M} = 0.4 \mu \text{sec}$$

interfacing I/O devices

①

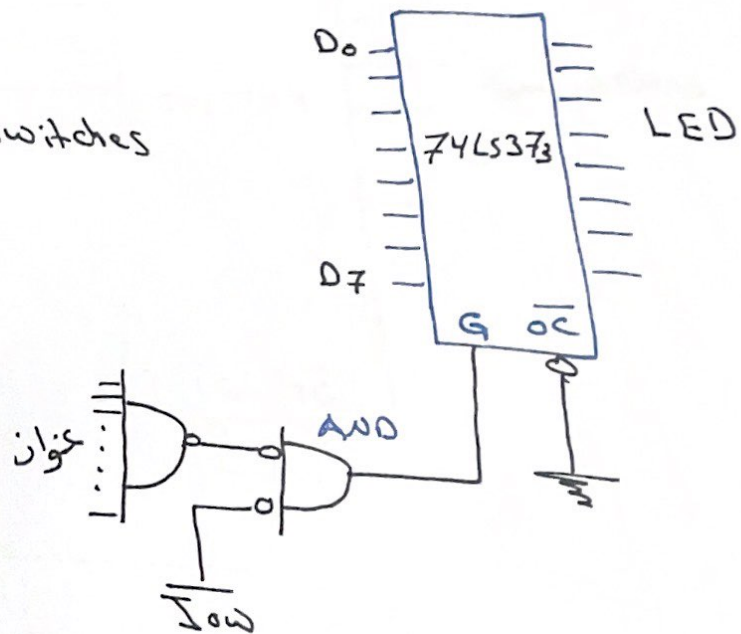
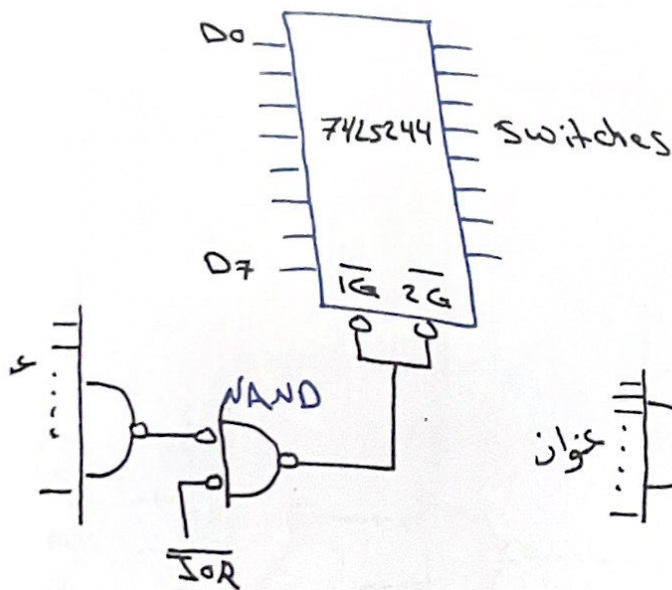
input Devices

- Switches
- $\overline{IOR}$
- 74LS244 Ics
- ➔ IN AL, Port no.



output Devices

- LED
- 7 segment Display
- $\overline{IOW}$
- 74LS374 IC's or 74LS373 IC's
- ➔ OUT Port no., AL



if Port no. is

98H

∴

8	4	2	1
A ₇	A ₆	A ₅	A ₄
1	0	0	1
<u>9</u>			

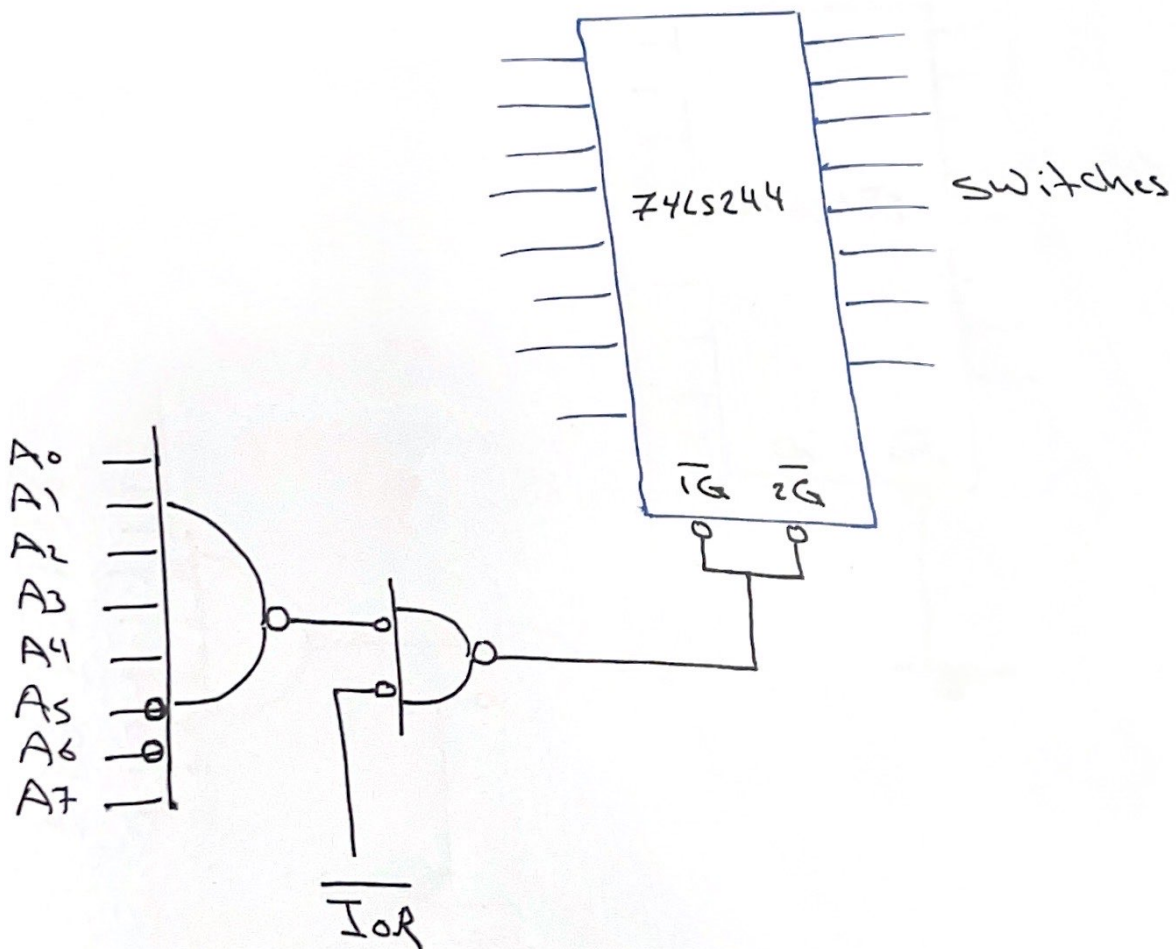
8	4	2	1
A ₃	A ₂	A ₁	A ₀
1	0	0	0
<u>8</u>			

Q2) Show the design of (IN AL, 9FH) by using 74LS244

ans

∴ Port no is 9FH

$A_7 A_6 A_5 A_4$	$A_3 A_2 A_1 A_0$
1 0 0 1	1 1 1 1



Q Show The Design of (OUT 99H AL)
using 74LS373

(3)

ans

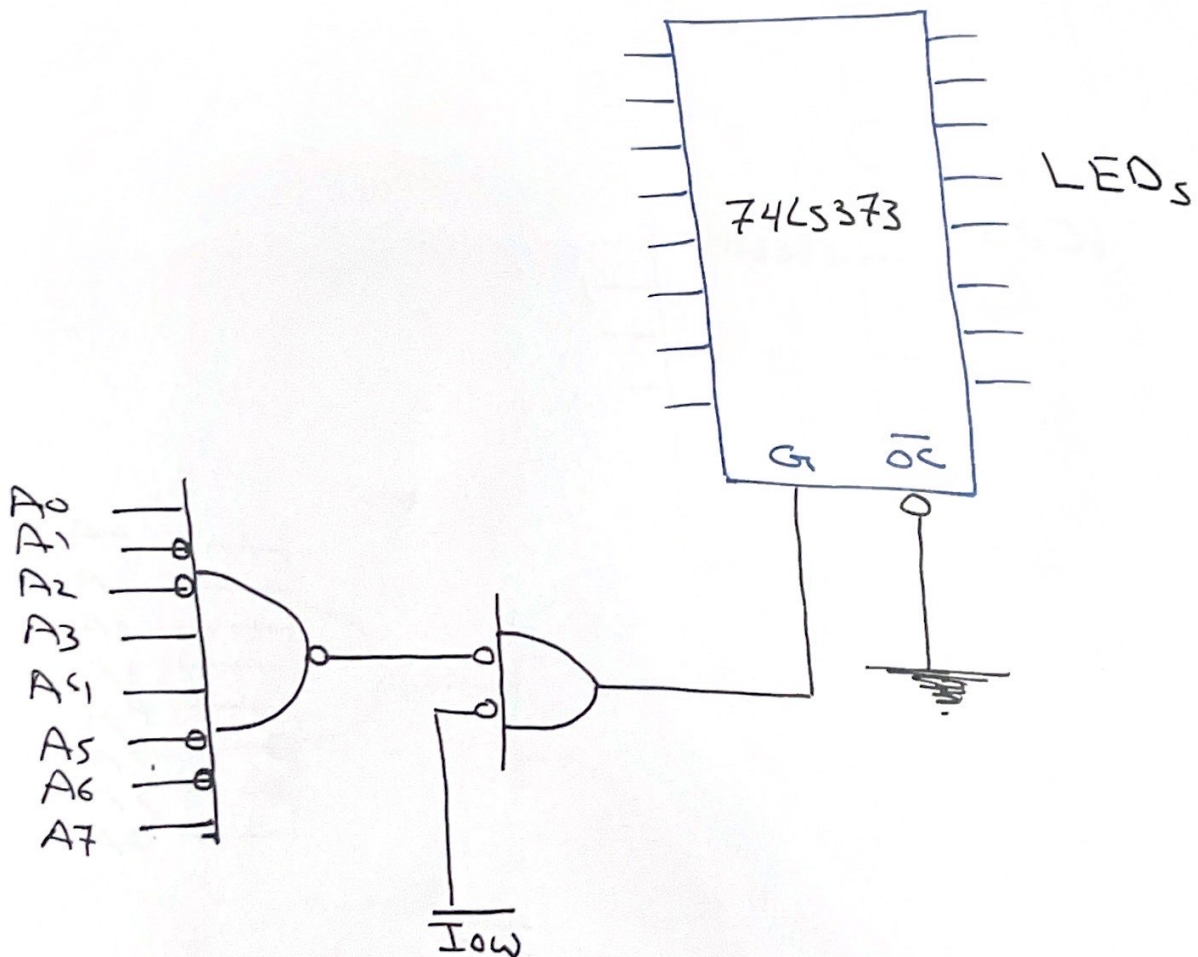
Port no = 99H

$A_7 A_6 A_5 A_4$

1 0 0 1

$A_3 A_2 A_1 A_0$

1 0 0 1

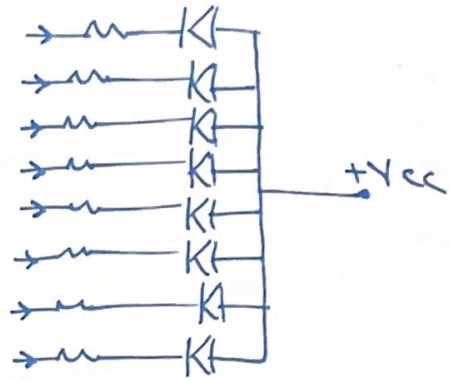
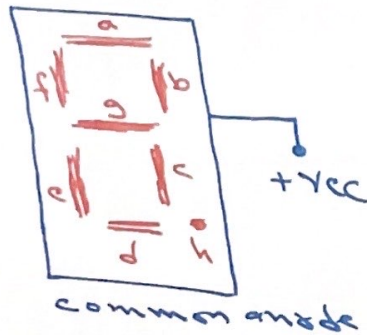


note

Display

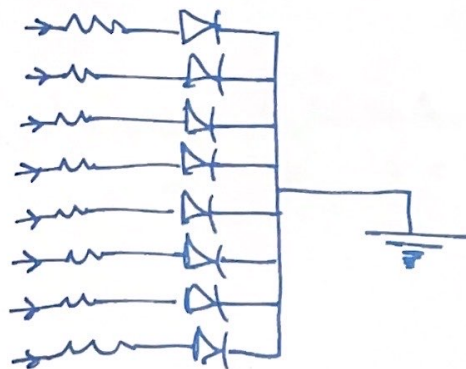
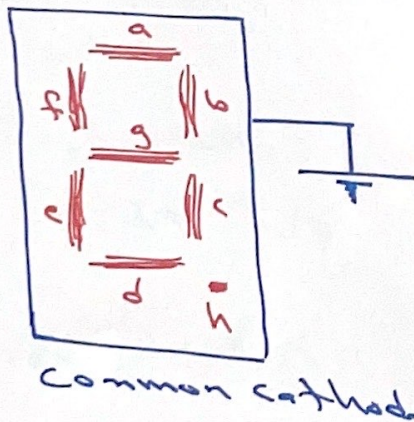
common anode

logic 0 LED on
logic 1 LED off



Common Cathode

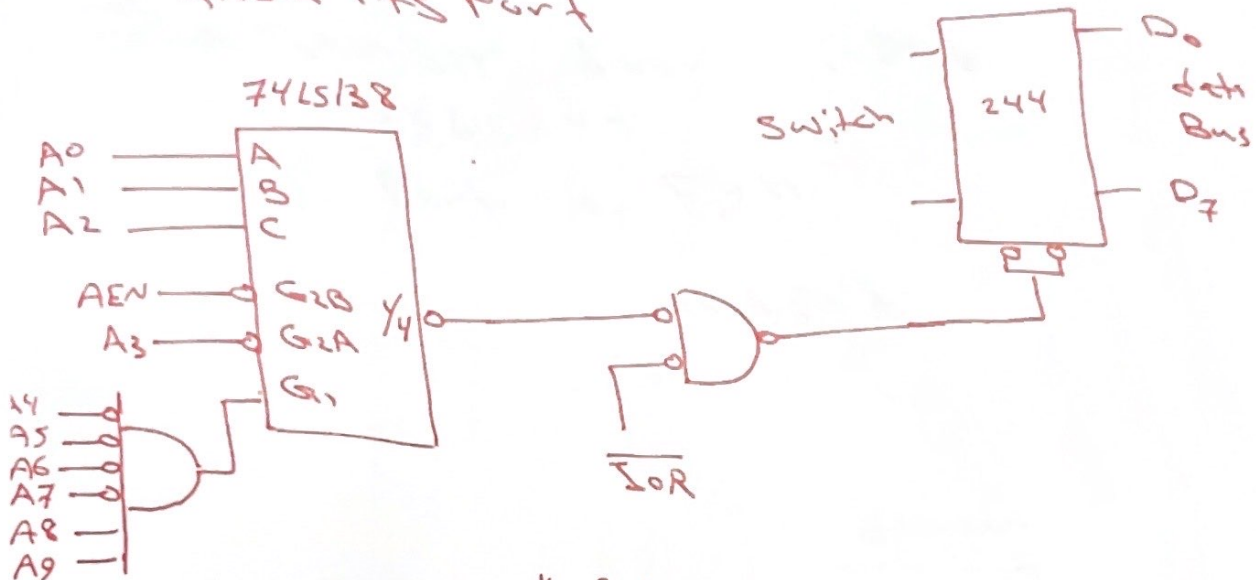
logic 0 LED off
logic 1 LED on



Ex for given block diagram find

6

- ① its address
- ② type of I/O interfacing
- ③ write instruction to ~~output~~ ^{read} Data from its Port



Ans :: Y_4

$\begin{matrix} 4 & 2 & 1 \\ C & B & A \\ A_2 & A_1 & A_0 \\ 1 & 0 & 0 \end{matrix}$

$A_3 = 0$

① address = 304H

$\begin{matrix} 2 & 1 \\ A_8 & A_7 \\ 1 & 1 \end{matrix}$ $\begin{matrix} 2 & 4 & 2 & 1 \\ A_7 & A_6 & A_5 & A_4 \\ 0 & 0 & 0 & 0 \end{matrix}$

$\begin{matrix} 2 & 4 & 2 & 1 \\ A_3 & A_2 & A_1 & A_0 \\ 0 & 1 & 0 & 0 \end{matrix}$

② :: $\overline{IOR}$, Switch, 7425244

$\therefore$ input I/O interfacing

③

mov DX, 304H

IN AL, DX

Q. Design security system for car door when it is open an alarm will be activated

ans $\rightarrow$ Sensor door input

74LS244

Ref Port no. F9H

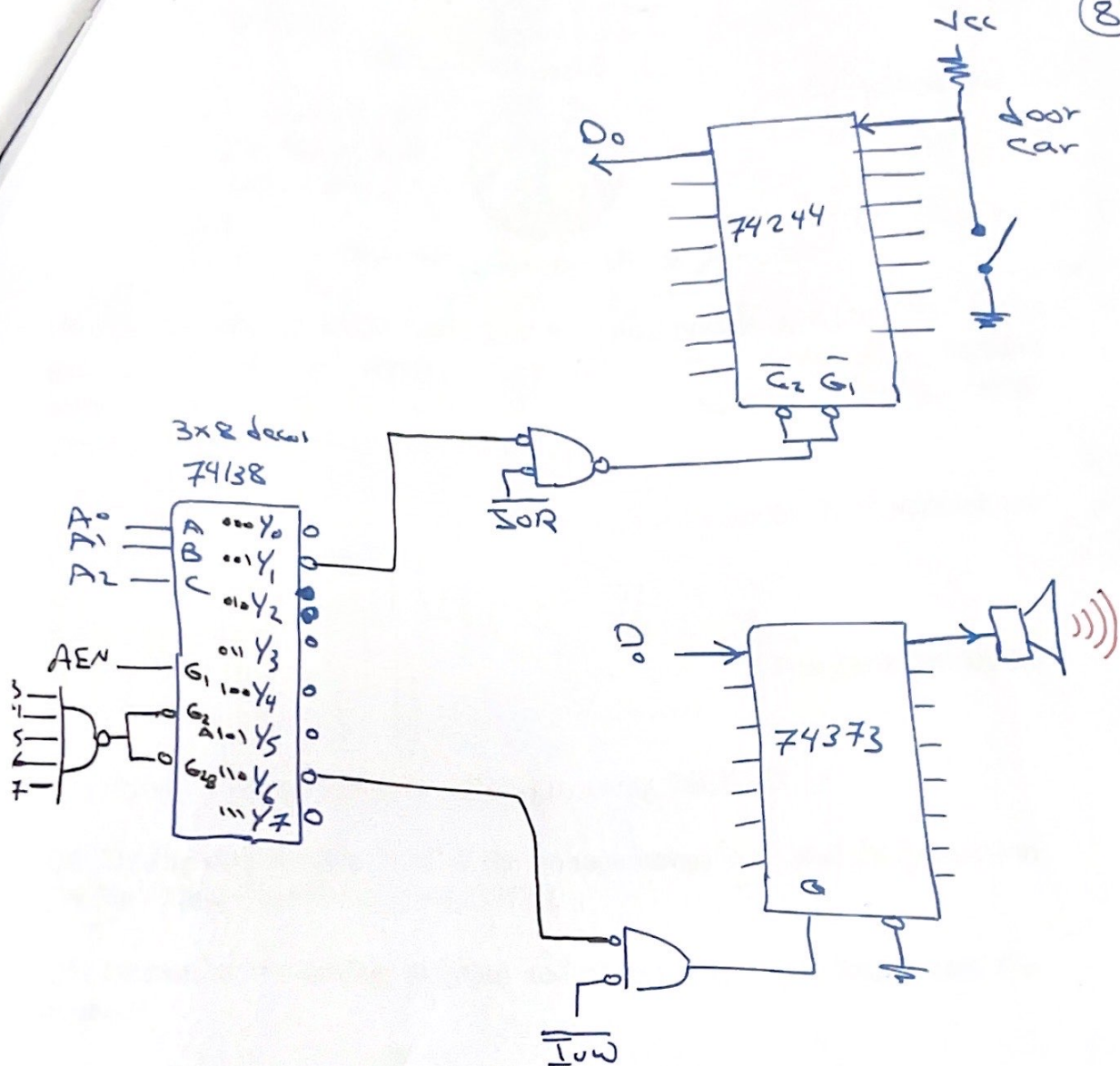
→ alarm output

74 LS 373

Left Port no

[illegible]

8



```
AGAIN: IN AL, F9
      RRC
      JC alarm
      JMP AGAIN
```

```
alarm: MOV AL, 01H
      OUT FE, AL
```

xxxxx xxxxx

كلية المأمون الجامعة

النظام الدراسي : السنوي
المادة : الزمن الحقيقي
الزمن : ثلاث ساعات



القسم: هندسة تقنيات الحاسوب

المرحلة: الثالثة

الإجابة على أربعة أسئلة

الامتحان النهائي للدور الأول للعام الدراسي (2020-2021)

Q1\ Design stepper motor controller by using port B of 8255 PPI where port A (B5H) and control register(85H), then write the required instructions for rotate the motor (90°) counter clockwise, (NT=100, motor speed 12RPM, CPU frequency= 1MHz).

90°
360
100
360

Q2\ 8254 PTI used to generate signal with duty cycle 20% answer the following:

- 1- find the control word for programming PTI.
- 2- find the frequency output if GATE1=1, CLK1=2MHz.
- 3- write the required instruction for programming 8254 to generate signal with duty cycle 80% if addressing range 70H-73H.

Q3\ show the design of (OUT 9F,AL) by using 74LS373.

Q4\ Design digital ramp ADC if the voltage range (5V) and the resolution (19.5mV) and filter frequency (200Hz).

Q5\ Determine the analog diagram and circuit diagram to implement the equation

$$V_o = -V_1 - 10V_2 + V_3 + 10V_4$$

10 A
11 B
12 C
13 D
14 E



8 4 2 1
0 1 0 1
1 0 1 1
1 0 0 0
1 0 0 1

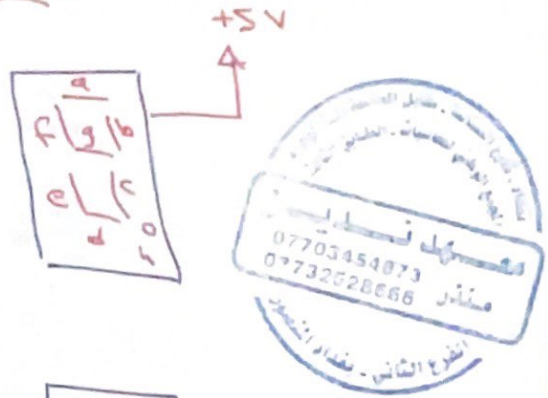
91

9 ← 2 0 1
8 ← 1 1 0
مدرس المادة: م. أحمد علي راضي

7 seven segment display

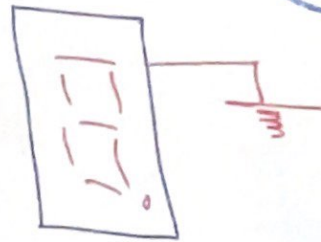
Common anode

0 → ON
1 → off



Common cathode

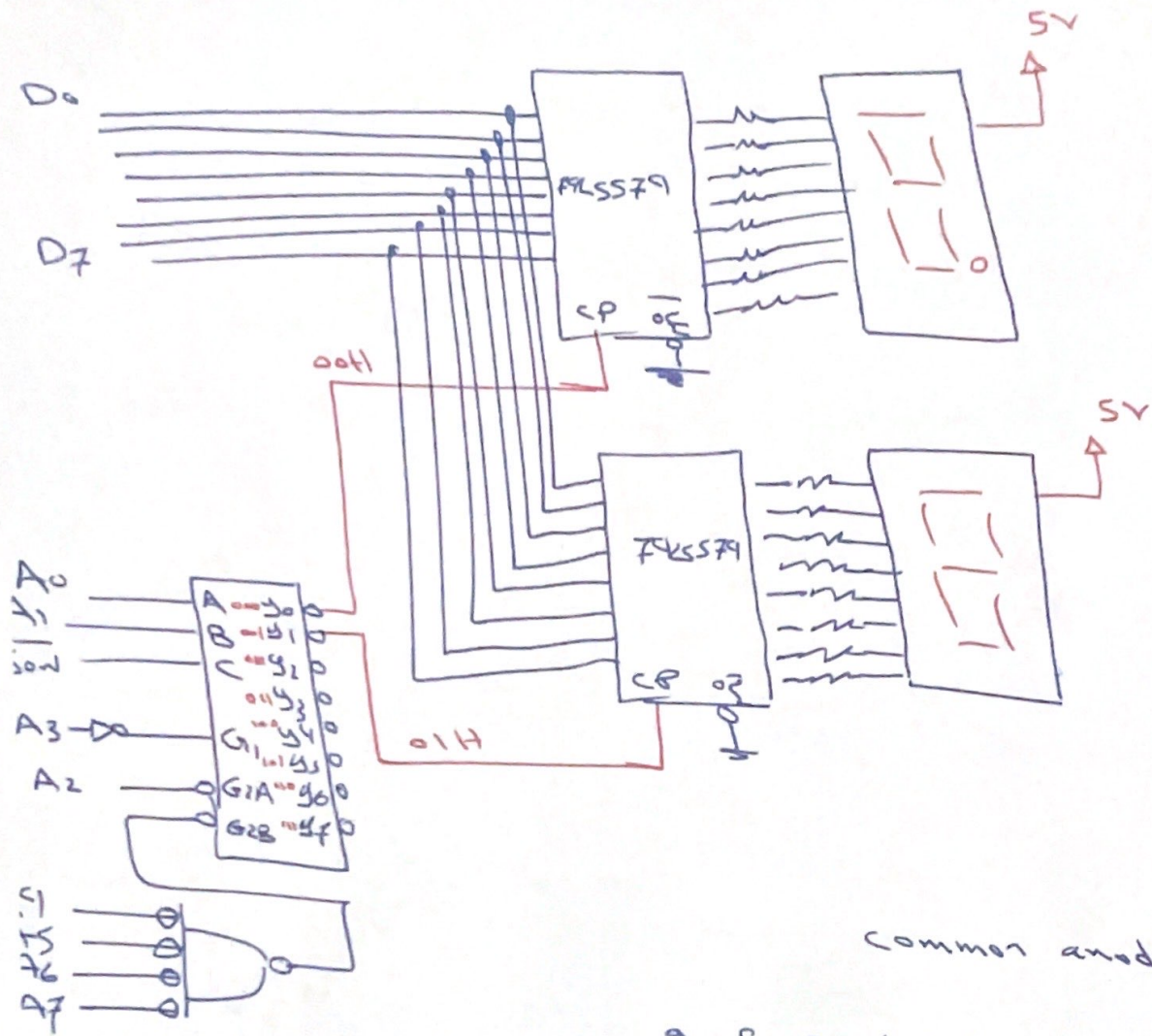
0 → off
1 → ON



Ex Design 8086 MPU interfacing circuit with Two 7-segment at the address $A_0=0$ and $A_0=1$ then write instruction to display No 98 on it

ans
∴ two 7 segment

	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	1



Common anode

g	f	e	d	c	b	a	h	a
0	0	1	0	0	0	0	0	f ₁₂₁₀
								e ₁₁₀
								d ₁₀₀
								c ₀₁₁
								b ₁₁₀
								a ₁₁₁
								h ₁₁₁

```

MOV AL, 20H
OUT 00H, AL
MOV AL, 00
OUT 01H, AL
INT 3
    
```

7 seven segment
a b c d e f g h

Q1 2017

3

answer the following based figure.1?

- ① find the address
- ② what changes if we use single decoder (use same address)
- ③ write the instruction for display No. (29)

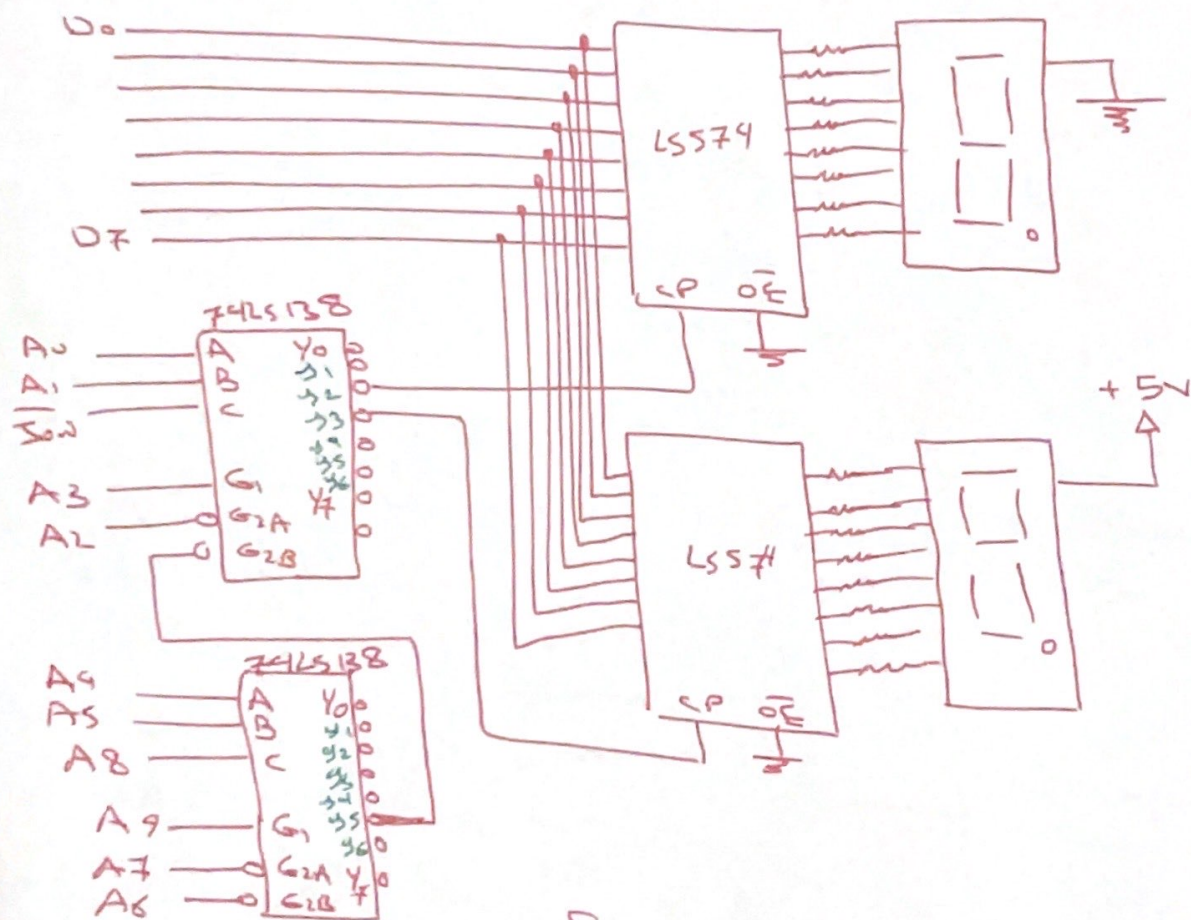


Figure 1

④

ans

① Seven Segment no. 1

$\overline{S_0} A_1 A_0$
0 1 0

$A_3 = 1$

$A_2 = 0$

$A_8 A_5 A_4$
1 0 1

seven segment no. 2 $\overline{S_3}$
 $\overline{S_0} A_1 A_0$
0 1 1

$A_9 = 1$
 $A_7 = 0$
 $A_6 = 0$

31AH

² A_9	¹ A_8	² A_7	⁴ A_6	² A_5	¹ A_4	² A_3	⁴ A_2	² A_1	¹ A_0
1	1	0	0	0	1	1	0	1	0

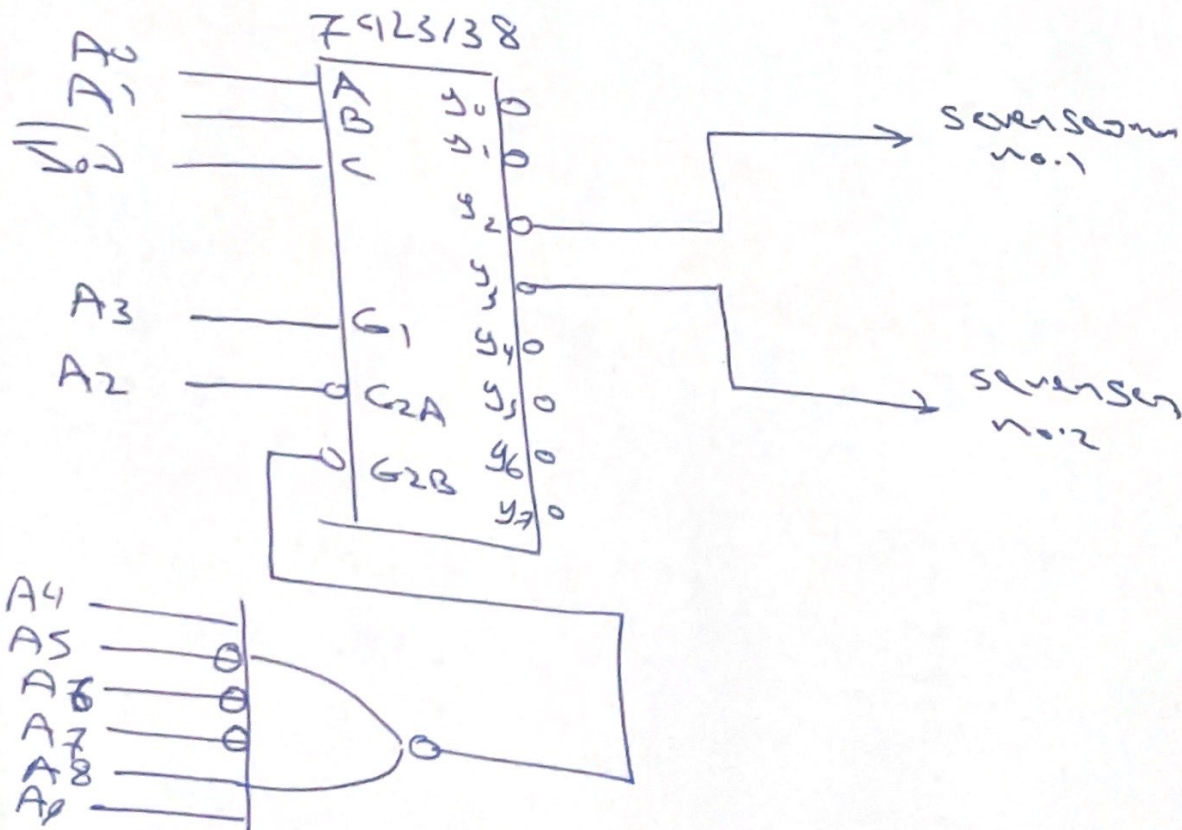
31BH

1	1	0	0	0	1	1	0	1	1
---	---	---	---	---	---	---	---	---	---

$\therefore$ two address

31AH & 31BH

②



③

no. 29

no. 2

Common cathod

a b c d e f g h
 1 1 0 1 1 0 1 0
 D A

DAH

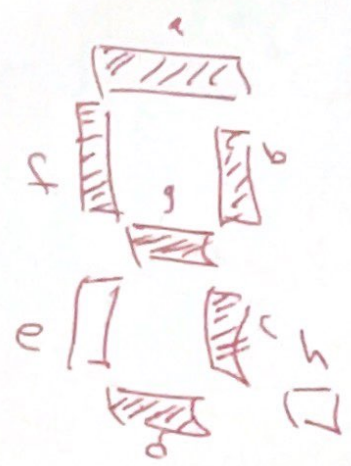


no. 9

Common anode

a b c d e f g h
 0 0 0 0 1 0 0 1
 0 9

09H



```
mov AL, DAH
mov DX, 31AH
out DX, AL
```

} Display no
 29

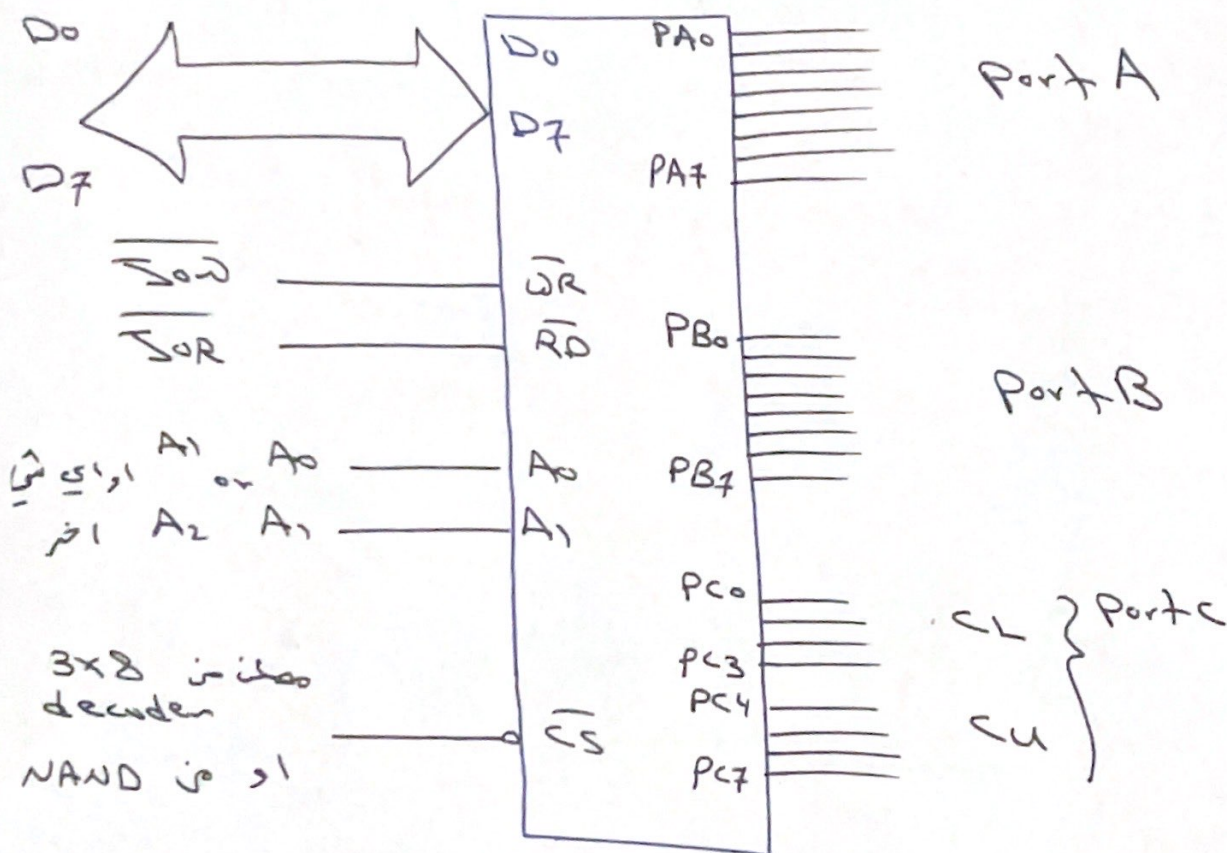
```
mov AL, 09H
mov DX, 31BH
out DX, AL
```

} Display no
 9

```
INT 3
```

6

lecture-5- 8255 Programmable Peripheral Interface PPI



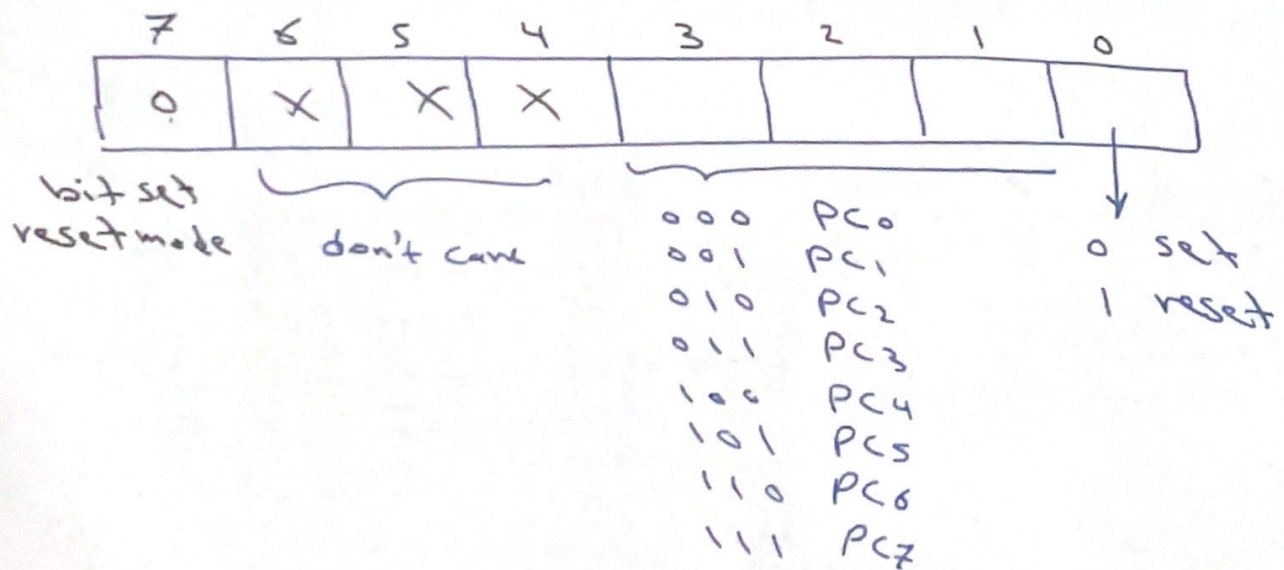
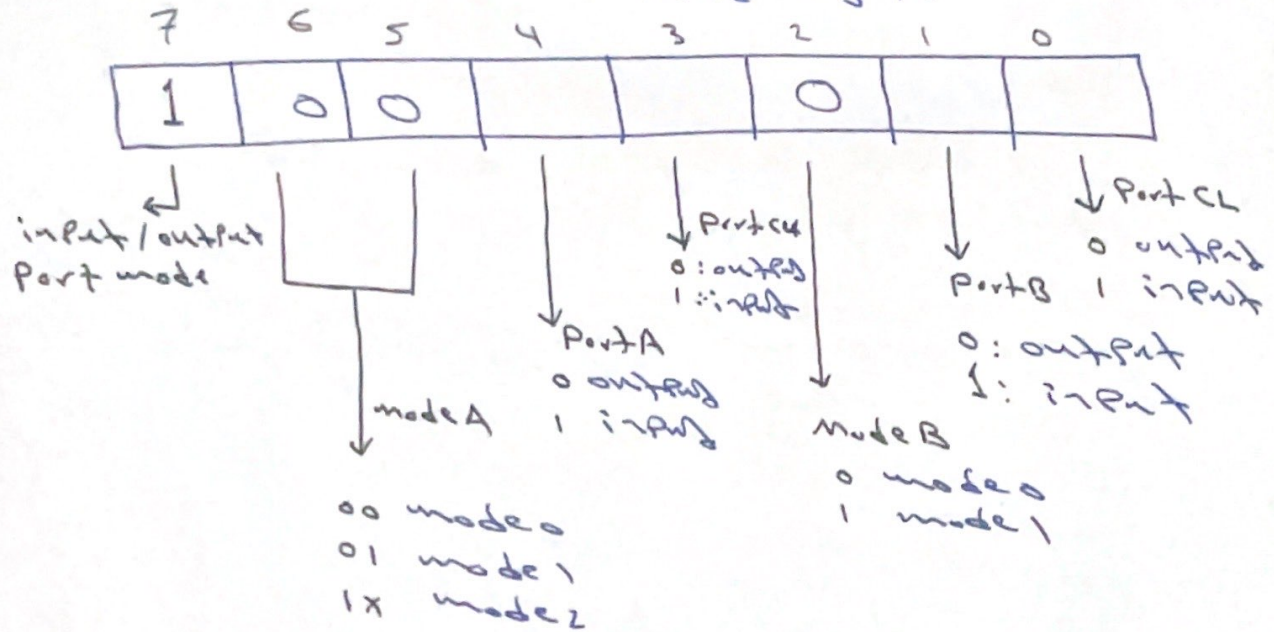
Three Port $\rightarrow$ Port A 8 bit
 $\rightarrow$ Port B 8 bit
 $\rightarrow$ Port C 8 bit
 Control word register

عنوان	A1A0
Port A	00
Port B	01
Port C	10
Control word	11

Control word Register

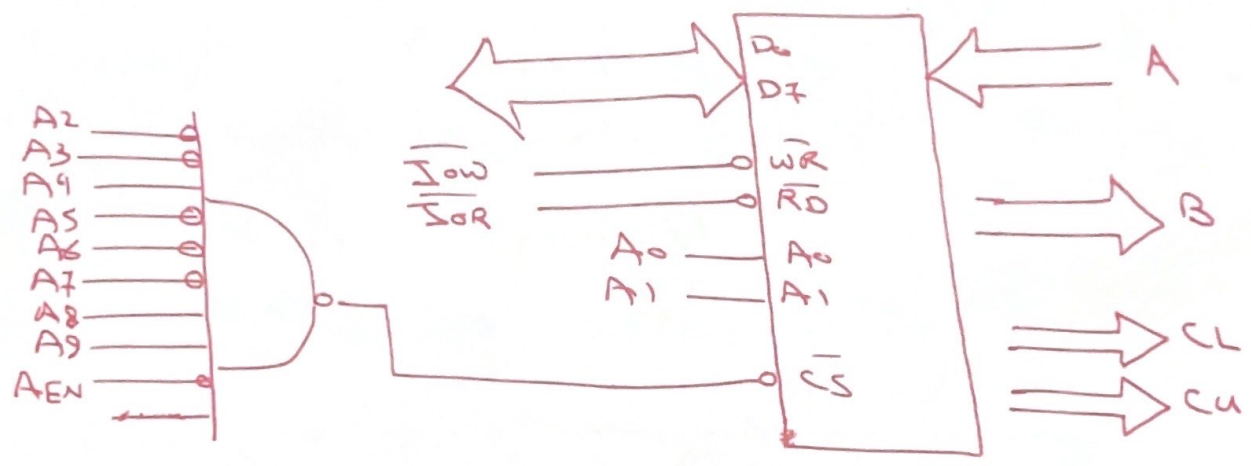
⑦

Command byte



Ex The 8255 in figure below is configured

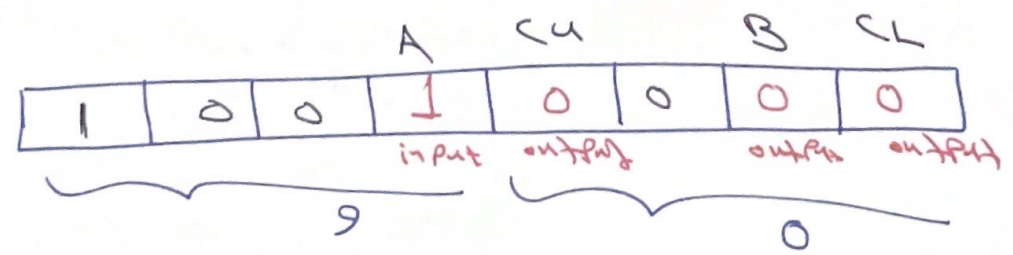
- ① find the Port address assigned to A, B, C and control word
- ② find the control byte (word) for this configuration
- ③ Program the ports to input data from Port A and send it to both port B and C



ans
①

Port		A ₉ A ₈	A ₇ A ₆ A ₅ A ₄	A ₃ A ₂ A ₁ A ₀
Port A	310H	1 1	0 0 0 1	0 0 0 0
Port B	311H	1 1	0 0 0 1	0 0 0 1
Port C	312H	1 1	0 0 0 1	0 0 1 0
Control	313H	1 1	0 0 0 1	0 0 1 1

②



∴ control word is 90H

```

mov AL, 90H
mov DX, 313H
out DX, AL
mov DX, 310H
in AL, DX
mov DX, 311H
out DX, AL
mov DX, 312H
out DX, AL

```

or using equ

```

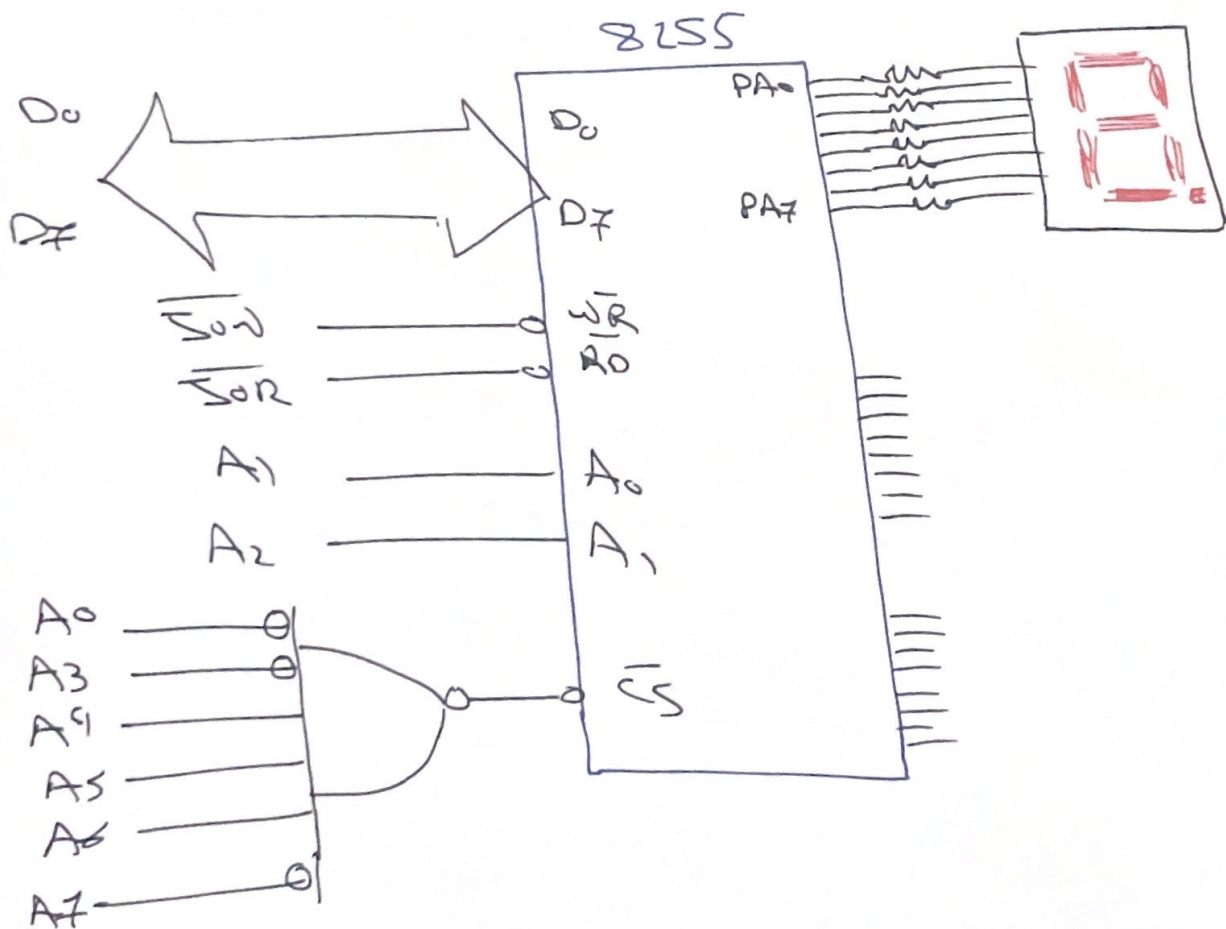
CTRLByte EQU 90H
PORTA EQU 310H
PORTB EQU 311H
PORTC EQU 312H
CTRLREG EQU 313H

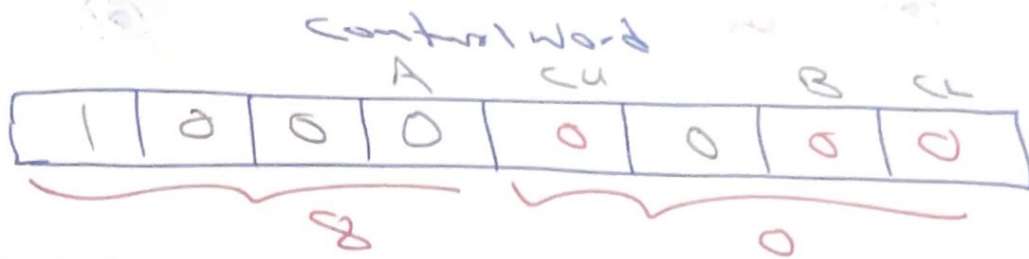
mov AL, CTRLByte
mov DX, CTRLREG
out DX, AL
mov DX, PORTA
in AL, DX
mov DX, PORTB
out DX, AL
mov DX, PORTC
out DX, AL

```

Q1 Design decimal counter by using 8255 display on 7-segment where Port address (PA = 70H, PB = 72H, PC = 74H, Control = 76H).

		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
PA	70H	0	1	1	1	0	0	0	0
PB	72H	0	1	1	1	0	0	1	0
PC	74H	0	1	1	1	0	1	0	0
Carry	76H	0	1	1	1	0	1	1	0





mov AL, 80H

out 76H, AL

start: mov CX, 10

mov AL, 0

again: out 70H, AL

INC AL

DEC CX

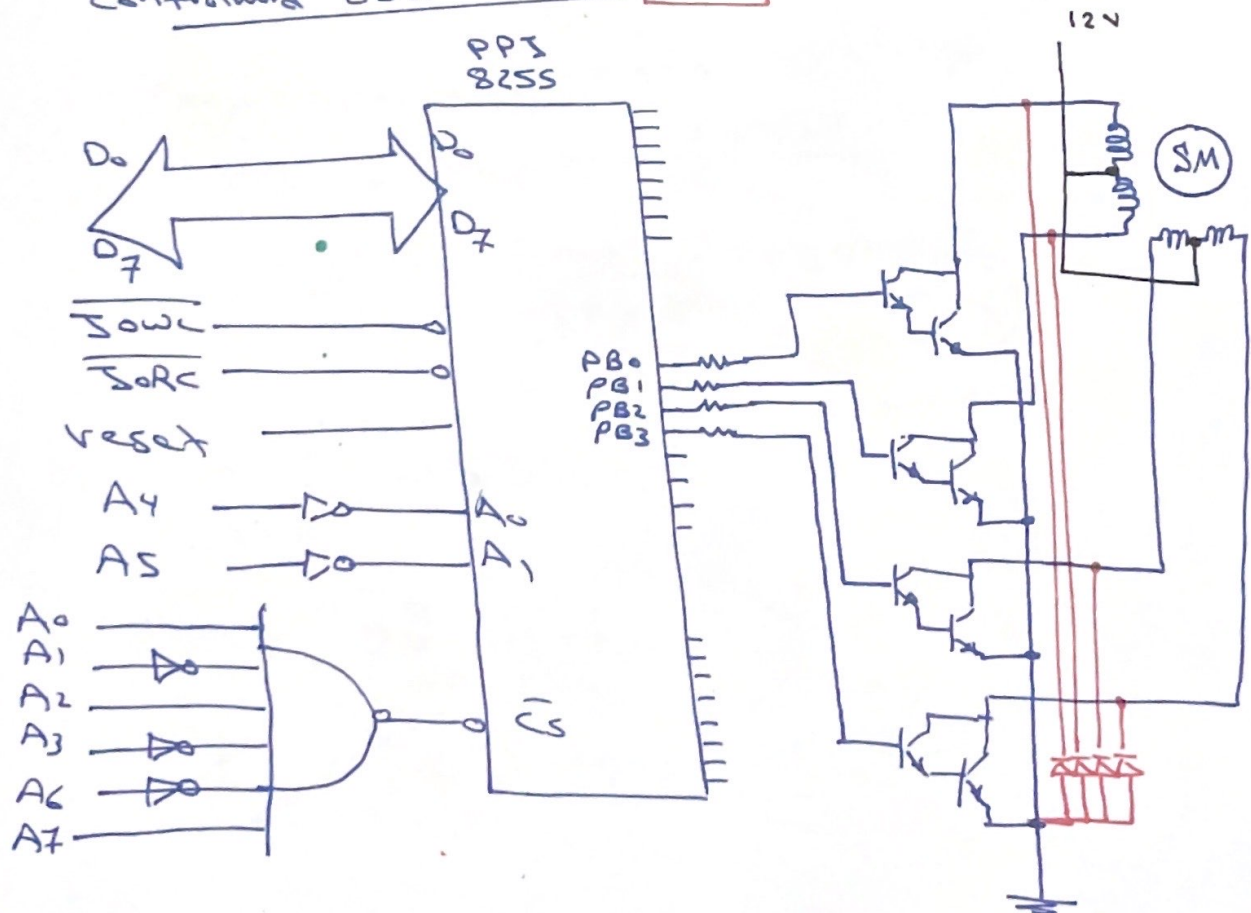
JNZ again

JMP start

① Design stepper motor controller by using Port B of 8255 PPI where Port A (B5H) and control word register (85H), then write the required instructions for rotate the motor (90°) counter clockwise NT=100, motor speed 12 RPM, CPU frequency = 1 MHz

ans

		A7	A6	A5	A4	A3	A2	A1	A0	
Port A	B5H	1	0	1	1	0	1	0	1	0
Port B	A5H	1	0	1	0	0	1	0	1	0
Port C	95H	1	0	0	1	0	1	0	1	0
Control word	85H	1	0	0	0	0	1	0	1	1



no. of teeth NT = 100

motor speed = 12 RPM

90° counter-clockwise

frequency = 1 MHz

$$\frac{12 \text{ RPM}}{60} = \frac{1}{5} \frac{\text{rotation}}{\text{sec}}$$

∴ 5 sec for each rotation

$$\therefore \frac{5 \text{ sec}}{100} = \underline{0.05 \text{ sec}} \text{ for each tooth}$$

$$\text{Clock Period} = \frac{1}{f} = \frac{1}{1\text{M}} = 1 \mu\text{sec}$$

loop instruction need 17 clock

$$\therefore \text{time of loop} = 17 * 1 \mu = \underline{17 \mu\text{sec}}$$

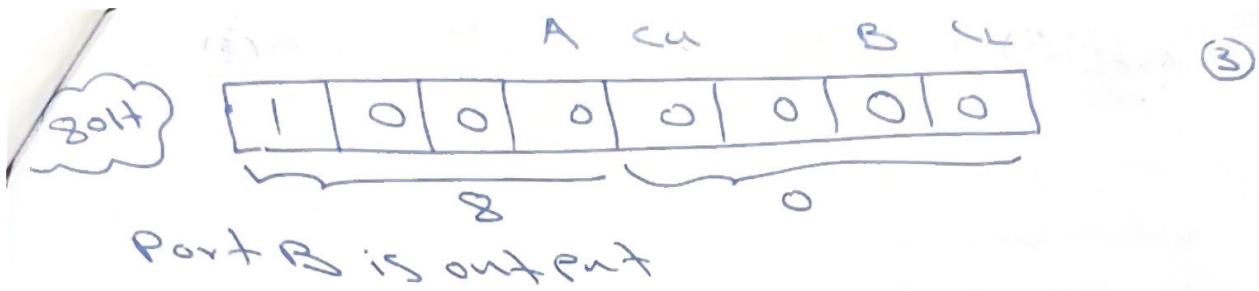
$$\therefore \frac{0.05 \text{ sec}}{17 \mu\text{sec}} = \frac{0.05}{17 \times 10^{-6}} = 2941.17$$

≈ 2941

$$\therefore \frac{360^\circ}{100} = 3.6^\circ$$

∴ only 90°

$$\therefore \frac{90^\circ}{3.6^\circ} = 25$$



MOV AL, 80H

OUT 85H, AL

; Program Port B output

MOV BL, 25

MOV AL, 33H

; initial position

back: OUT 85H, AL

ROL AL, 1

; Counter Clock wise

MOV CX, 2941

Self: LOOP Self

DEC BL

JNZ back

HLT

Q Design cross (4-way) traffic light system by using 8255 PPI, where the time of stop (Red) is 10sec, ~~then write~~ and time of wait (yellow) is (3 second) then write the required instruction of port A B5H control register 85H, and CPU frequency = 1MHz

ans

		A7A6	A5	A4	A3A2A1A0	
Port A	B5H	1	0	1	1	00
Port B	A5H	1	0	1	0	01
Port C	95H	1	0	0	1	10
control	85H	1	0	0	0	11

red $\rightarrow$ 10sec } green = red - yellow = 10 - 3 = 7sec
yellow $\rightarrow$ 3sec }

way 4	way 3	way 2	way 1	
R Y G	R Y G	R Y G	R Y G	
1 0 0	1 0 0	1 0 0	0 0 1	7sec
1 0 0	1 0 0	1 0 0	0 1 0	3sec
1 0 0	1 0 0	0 0 1	1 0 0	7sec
1 0 0	1 0 0	0 1 0	1 0 0	3sec
1 0 0	0 0 1	1 0 0	1 0 0	7sec
1 0 0	0 1 0	1 0 0	1 0 0	3sec
0 0 1	1 0 0	1 0 0	1 0 0	7sec
0 1 0	1 0 0	1 0 0	1 0 0	3sec

6

Q₅ stepper motor interface with 8255 PPT
answer the following:

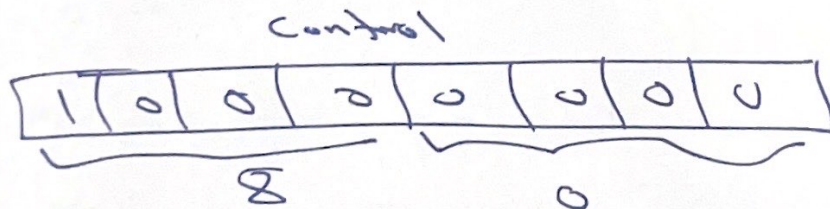
- 1- find Port address if A₅-A₀ connected to chipselect pin
- 2- Design the interfacing circuit if the motor interfaced with Port B
- 3- write the required instruction for rotating motor counter clockwise motor speed = 12 RPM and CPU frequency = 1 MHz

ans

①

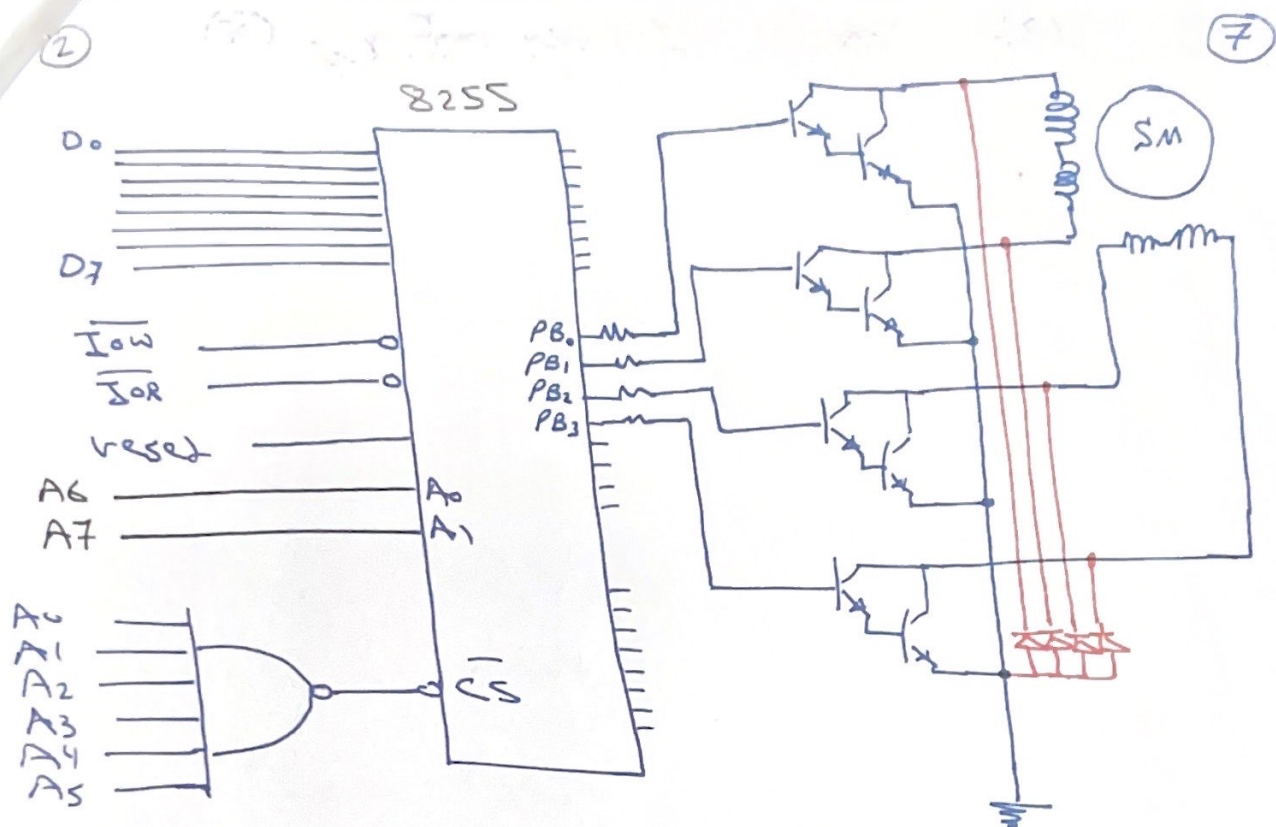
		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
Port A	3FH	0	0	1	1	1	1	1	1
Port B	7FH	0	1	1	1	1	1	1	1
Port C	BFH	1	0	1	1	1	1	1	1
Control word	FFH	1	1	1	1	1	1	1	1

باركان كتابه
فتح ثابت لانه
لم يذكر قيعال



8017

Port B output



③

∴ Speed 12 RPM

$$\frac{12}{60} = \frac{1}{5} \frac{\text{rotation}}{\text{sec}}$$

∴ 5 sec for each rotation

Let stepper motor ~~NT~~ = 100

$$\frac{5}{100} = 0.05 \text{ sec}$$

$$\text{clock period} = \frac{1}{F} = \frac{1}{1M} = 1 \mu \text{ sec}$$

$$\text{loop period} = 17 \times 1 \mu = 17 \mu \text{ sec}$$

$$\text{Period for one step} = \frac{0.05}{17 \mu} = \underline{\underline{2941}}$$

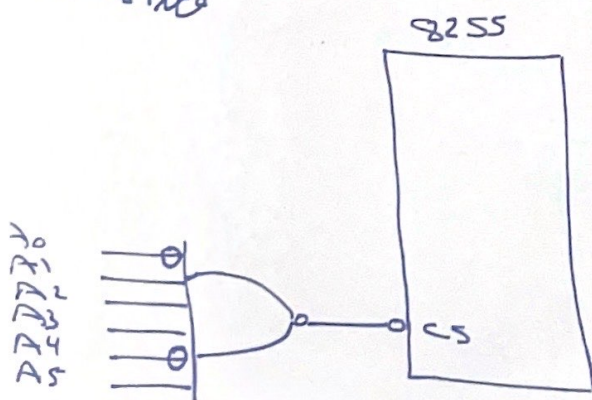
```
MOV AL, 80H
OUT FFH, AL
MOV AL, 33H
again: OUT 7FH, AL
      ROL AL, 1
      MOV CX, 2941
here:  loop here
      JMP again
```

Continuous rotating stepper motor counter
clock wise

20x10

if $A_5 - A_0 = 101110$

over life

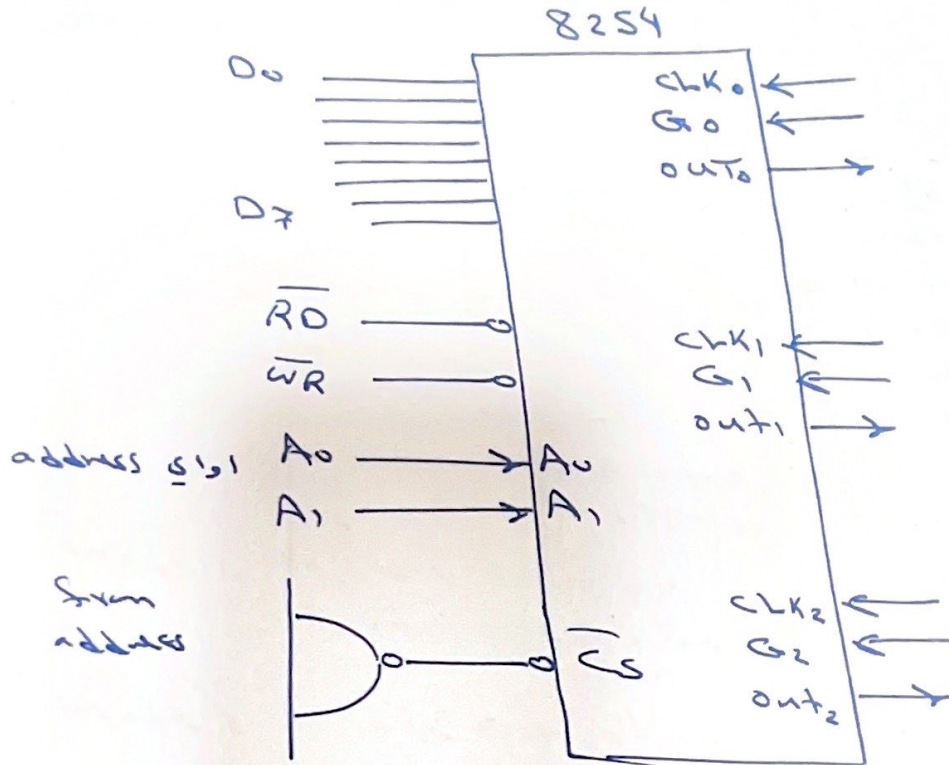


lecture - 6 -

Programmable interval timer

8254
8253

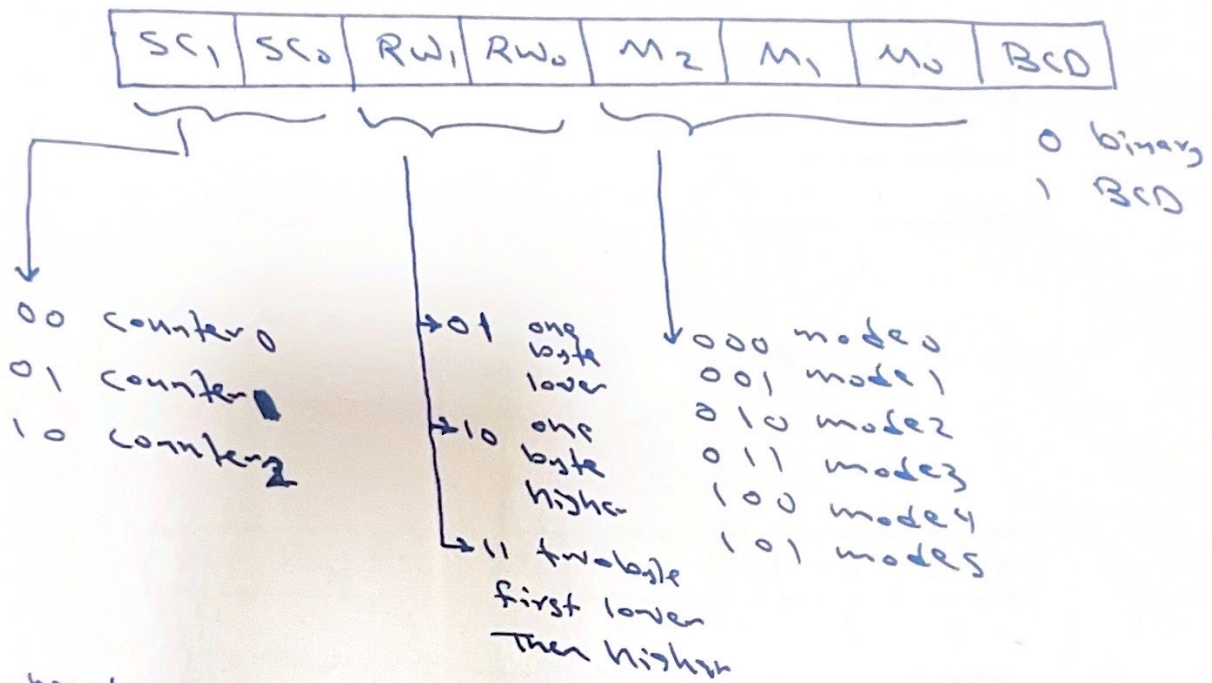
①



	A ₁ A ₀
Counter 0	0 0
Counter 1	0 1
Counter 2	1 0
Control word	1 1

Control Word

(2)



mode 0 event counter
interrupt or terminal count

mode 2 : Rate generator
continuous pulses



mode 3 : Square wave
rate generator



Ex 5.1 $\overline{CS}$ A7-A2 = 100101

(a) Find port address assign for 8253/8254

(b) Find the configuration 8254 if the control register programmed as follows

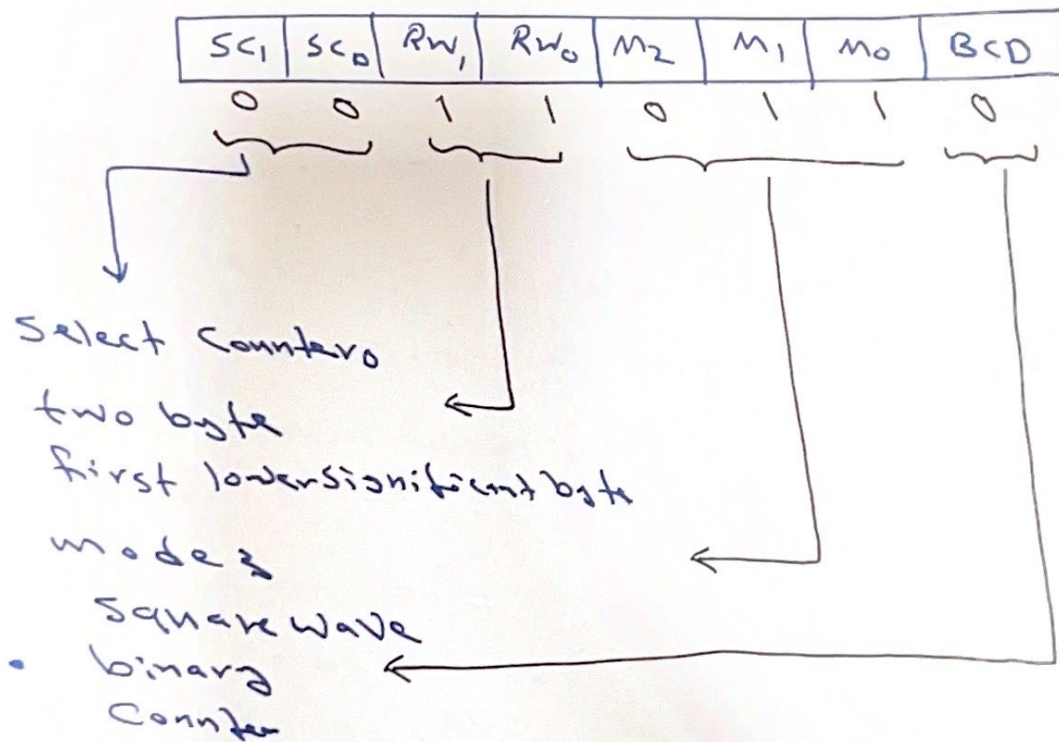
MOV AL, 00110110

OUT 97H, AL

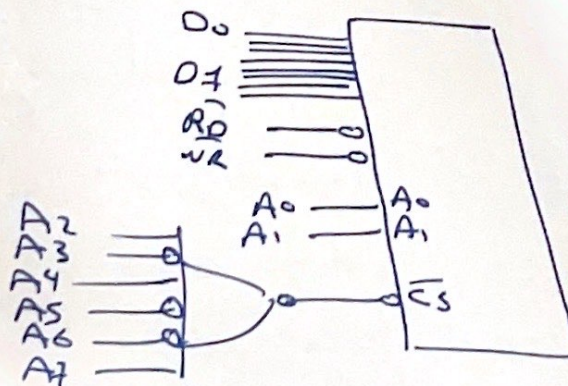
ans = (a)

		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
Counter 0	94H	1	0	0	1	0	1	0	0
Counter 1	95H	1	0	0	1	0	1	0	1
Counter 1	96H	1	0	0	1	0	1	1	0
Control Word	97H	1	0	0	1	0	1	1	1

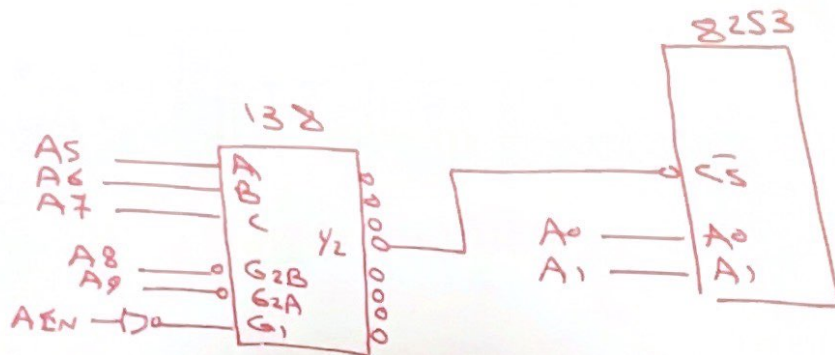
(b) `mov AL, 00110110`
`out 97H, AL`



note



Ex Find port address & counter address



ans = $\frac{1}{2} = \begin{matrix} C & B & A \\ 0 & 1 & 0 \\ A_7 & A_6 & A_5 \end{matrix}$

		A ₉ A ₈	A ₇ A ₆	A ₅ A ₄	A ₃ A ₂ A ₁ A ₀
Counter 0	40H	00	010X	XX00	
Counter 1	41H	00	010X	XX01	
Counter 2	42H	00	010X	XX10	
Control register	43H	00	010X	XX11	

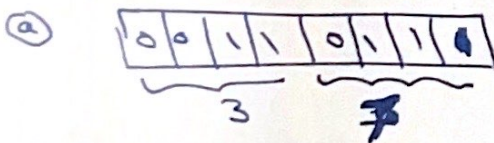
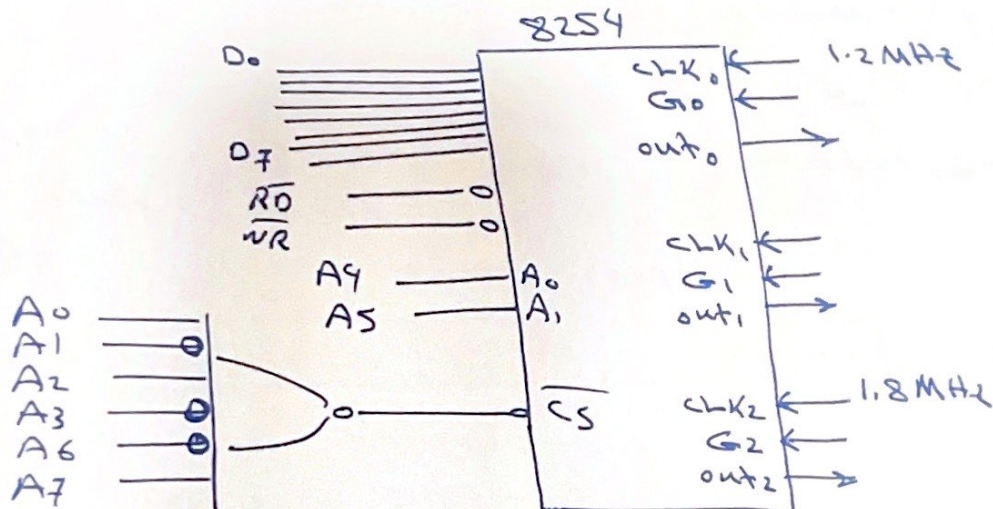
Q Design a timer circuit using 8254 with using counter 0 (B5H) and control using (85H) then write a program

- Counter 0 for binary count of mode 3 to divide clock by 910. (4282)BCD
- Counter 2 for binary count of mode 3 to divide CLK₂ by number C26A Hex
- Find the frequency output from out₀ and out₂ in @ 80 if CLK₀ = 1.2 MHz CLK₂ = 1.8 MHz

ans

(5)

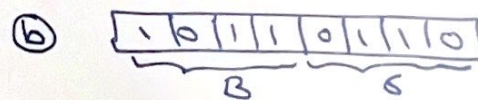
		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
counter 0	B5H	1	0	1	1	0	1	0	1
counter 1	A5H	1	0	1	0	0	1	0	1
counter 2	95H	1	0	0	1	0	1	0	1
Control Register	85H	1	0	0	0	0	1	0	1



```

mov AL, 37H
mov 85H, AL
mov AL, 82H
out 85H, AL
mov AL, 42H
out 85H, AL
HLT

```



```

mov AL, B6H
out 85H, AL
mov AL, 6AH
out 95H, AL
mov AL, C2
out 95H, AL
HLT

```

(c) $CLK_0 = 1.2M$ $N = 4282$ BCD $f_{out} = \frac{f_{CLK}}{N} = \frac{1.2 \times 10^6}{4282} = 280 Hz$

$CLK_2 = 1.8M$ $N = C26A Hex \rightarrow 49770$

$f_{out} = \frac{f_{CLK}}{N} = \frac{1.8 \times 10^6}{49770} = 36 Hz$

Q2 8254 PPI used to generate signal with duty cycle 20%. answer the following

- 1- find the control word for Programming PPI
- 2- find the frequency output if $GATE_1 = 1$

$CLK_1 = 2 MHz$

- 3- write the required instruction for programming 8254 to generate signal with duty cycle 80% if addressing range 70H-73H

ans

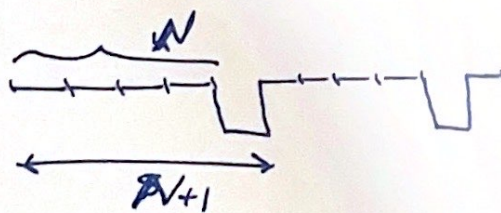
control register

SC ₁	SC ₀	0	1	M ₂	M ₁	M ₀	BCD
-----------------	-----------------	---	---	----------------	----------------	----------------	-----

0 1
counter

0 1 0 0
mode 2
continuous pulse $\neq 50\%$

80% duty cycle



or
Duty cycle = $\frac{N}{N+1} = 80\%$

$$\frac{N}{N+1} = 0.8$$

$$N = 0.8N + 0.8$$

$$N - 0.8N = 0.8$$

$$0.2N = 0.8$$

$$N = \frac{0.8}{0.2} = 4$$

$\therefore$ only one byte

$\therefore$ ① control word

01010100
5 4

$\therefore$ control word = 54H

② $f_{out} = \frac{CLK}{N} = \frac{2M}{4} = 0.5MHz$
 $= 500kHz.$

③

Counter 0	70H
Counter 1	71H
Counter 2	72H
Control register	73H

```

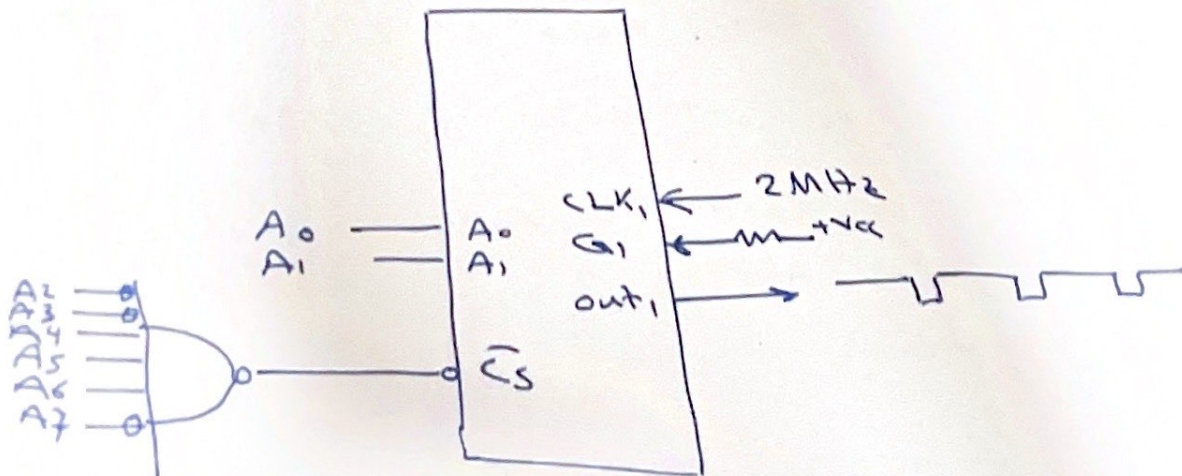
MOV AL, 54H
OUT 73H, AL

MOV AL, 04
OUT 71H, AL

HLT
  
```

if Design

	A ₇ A ₆ A ₅ A ₄	A ₃ A ₂ A ₁ A ₀
70	0 1 1 1	0 0 0 0
71	0 1 1 1	0 0 0 1
72	0 1 1 1	0 0 1 0
73	0 1 1 1	0 0 1 1

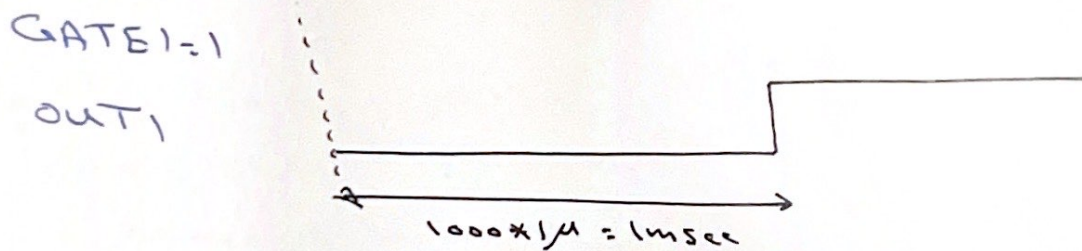


S-7
Ex assume $GATE1=1$ $CLK=1MHz$
 Count $N=1000$. Show the output of
 out₁ if the it is programmed mode 0

ans
 $\therefore$ mode 0

$$\therefore T = \frac{1}{f} = \frac{1}{1M} = 1\mu sec$$

$\therefore$ output Low for $NT = 1000 \times 1\mu = 1000\mu sec$
 $= 1msec$
 and then remain high

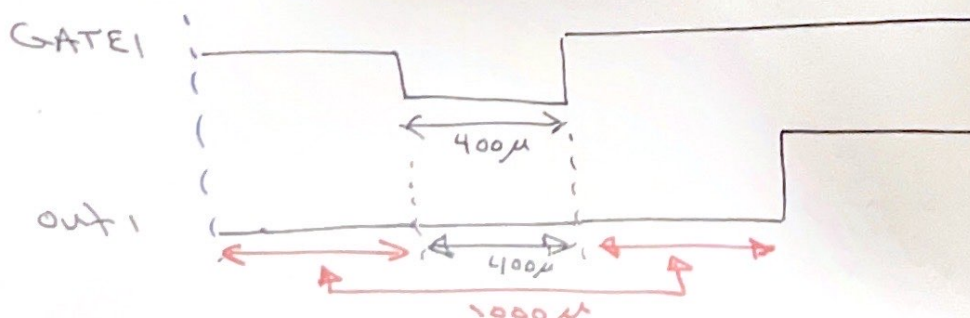


Ex assume $GATE1$ becomes zero for $400\mu s$
 what is the width of the low pulses for
 out₁ in Ex 5-7

ans $\therefore NT = 1000 \times 1\mu = 1000\mu sec$

$\therefore GATE1=0$ $400\mu sec$

$\therefore$ low output $\therefore 1000\mu + 400\mu sec$
 $= 1400\mu sec$



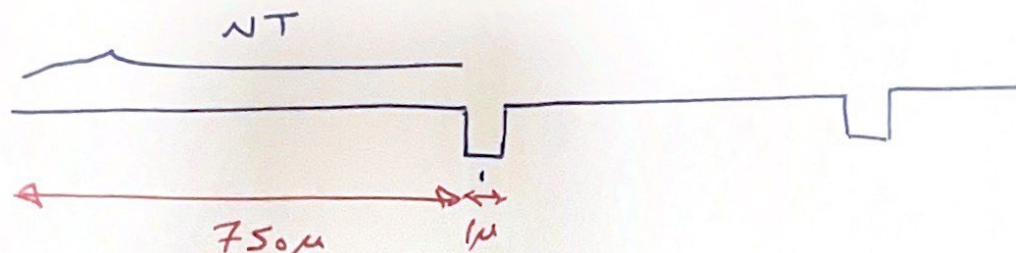
9

Ex 5-10 if $CLK_2 = 1\text{MHz}$ $GATE_2 = 1$

and $N = 750$ show out_2 if $count_2$ is programmed for mod 2

ans $T = \frac{1}{CLK} = \frac{1}{1\text{M}} = 1\mu\text{sec}$

mode 2

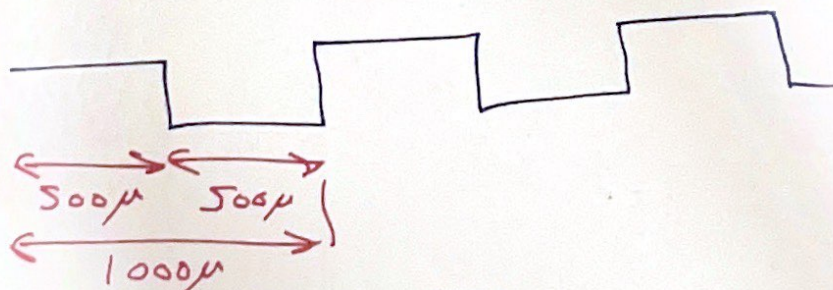


Ex if $CLK_2 = 1\text{MHz}$ $GATE_1 = 1$
 $N = 1000$ show out_1 if $count_1$ is
 Programmed for mode 3

ans $\therefore$ square wave $high = low = \frac{N}{2} = 500$

$T = \frac{1}{1\text{M}} = 1\mu\text{sec}$

$\frac{N}{2}T = \frac{1000}{2} \times 1\mu = 500\mu\text{sec}$



Ex if $CLK_2 = 1\text{MHz}$ $GATE_1 = 1$
 $N = 19$

ans $high = \frac{N+1}{2} = \frac{19+1}{2} = \frac{20}{2} = 10$

$low = \frac{N-1}{2} = \frac{19-1}{2} = \frac{18}{2} = 9$

