

كلية المأمون الجامعة
قسم هندسة تقنيات الحاسوب

الإلكترونيك ***ELECTRONICS***

المرحلة الثانية

الجزء الثاني - الفصلين : الثالث والرابع

الدكتور
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العام الدراسي ٢٠٢٣ – ٢٠٢٤

Chapter – 3

BJT (Bipolar Junction Transistor)

3-1: BJT Transistor DC Equivalent Circuits: Common Base, Common Collector, Common Emitter:

Transistor Types :

The main types of the transistor are shown in Fig.(3.1).

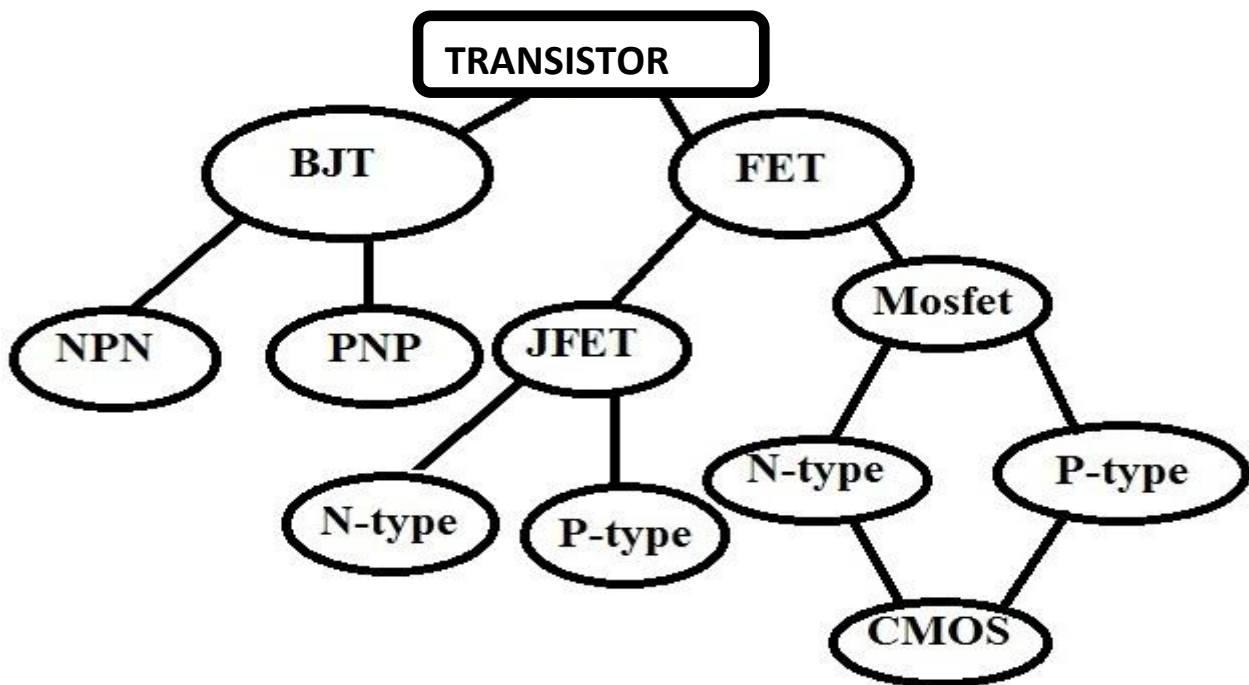


Fig. 3-1. Transistor Types

In this chapter , we will discuss the first types of transistors which is the **Bipolar Junction Transistor (BJT)**. The operation of the Bipolar (Bi $\equiv$ Two in Greek) Junction transistor (BJT) can be explained in terms of the two carriers , the electrons and holes (two-polarities) charge flow; the transistor is therefore called **bipolar**.

The operation of the field-effect transistor (FET) can be explained in terms of only majority-carrier (one-polarity) charge flow; the transistor is therefore called **Unipolar**. It will be discussed in the next chapter. Two kinds of field-effect devices are widely used: the junction field-effect transistor (JFET) and the metal-oxide-semiconductor field-effect transistor (MOSFET).

Basic Construction:[1]

The transistor is a three-layer semiconductor device consisting of either two n - and one p -type layers of material or two p - and one n -type layers of material. The former is called an ***NPN transistor***, while the latter is called a ***PNP transistor***. Both (with symbols) are shown in Fig. 3-2. The middle region of each transistor type is called the ***base (B)*** of the transistor. Of the remaining two regions, one is called ***emitter (E)*** and the other is called the ***collector (C)*** of the transistor. For each transistor type, a junction is created at each of the two boundaries where the material changes from one type to the other. Therefore, there are two junctions: ***emitter-base (E-B) junction*** and ***collector-base (C-B) junction***. The outer layers of the transistor are heavily doped semiconductor materials having widths much greater than those of the sandwiched p - or n -type material. The doping of the sandwiched layer is also considerably less than that of the outer layers (typically 10:1 or less). This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of "free" carriers.

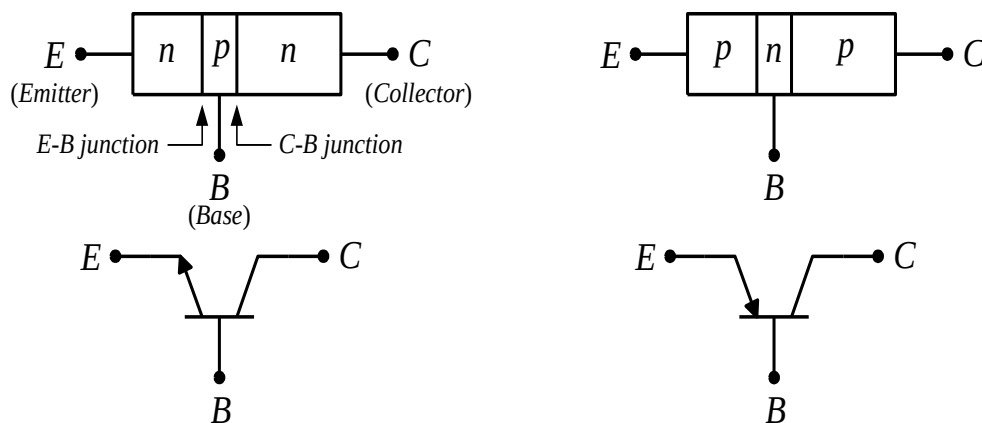


Fig. 3-2. The two types of BJT transistors

The dc biasing is necessary to establish the proper region of operation for ac amplification or switching purposes. Table 3-1 shows the transistor operation regions and the purpose with respect to the biasing of the E-B and C-B junctions.

[1]- From Dr.Muataz Al-Azawi Lectures, Al-Mamon University College , 2013

Table 3-1. The transistor operation regions

Operation region		Purpose	Junctions biasing	
			E-B junction bias	C-B junction bias
1	Active region	Amplification	Forward-biased	Reverse-biased
2	Cutoff region	Switching	Reverse-biased	Reverse-biased
3	Saturation region		Forward-biased	Forward-biased

Active Region Operation:

The basic operation of the transistor will now be described using the pnp transistor of Fig. 3-3. The operation of the npn transistor is exactly the same if the roles played by the electron and hole are interchanged. When the E-B junction is forward-biased, a large number of majority carriers will diffuse across the forward-biased p-n junction into the n-type material (base). Since the base is very thin and has a low conductivity (lightly doping), a very small number of these carriers will take this path of high resistance to the base terminal. The larger number of these majority carriers will diffuse across the reverse-biased C-B junction into the p-type material (collector). The reason for the relative ease with which the majority carriers can cross the reverse-biased C-B junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the n-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig. 3-3.

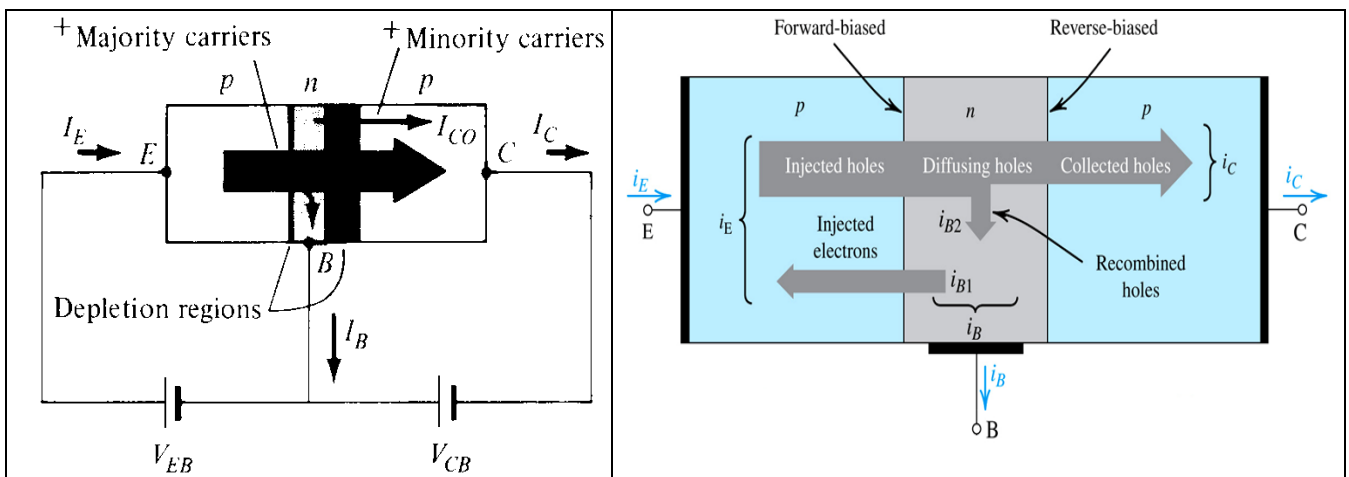


Fig. 3-3. The current flow in the transistor.

Applying Kirchhoff's current law to the transistor of Fig. 3-3, we obtain

$$I_E = I_C + I_B \quad [3.1]$$

The collector current, however, is comprised of two components: the majority and minority carriers as indicated in Fig. 3-3. The minority-current component is called the **leakage current** and is given the symbol I_{CO} (I_C current with emitter terminal Open). The collector current, therefore, is determined in total by Eq. [3.2].

$$I_C = I_{C \text{ majority}} + I_{CO \text{ minority}} \quad [3.2]$$

Common-Base (CB) Configuration:

The common-base configuration with NPN and PNP transistors are indicated in Fig. 3-4. The common-base terminology is derived from the fact that the base is common to both input and output sides of the configuration. In addition, the base is usually terminal closest to, or at, the ground potential.

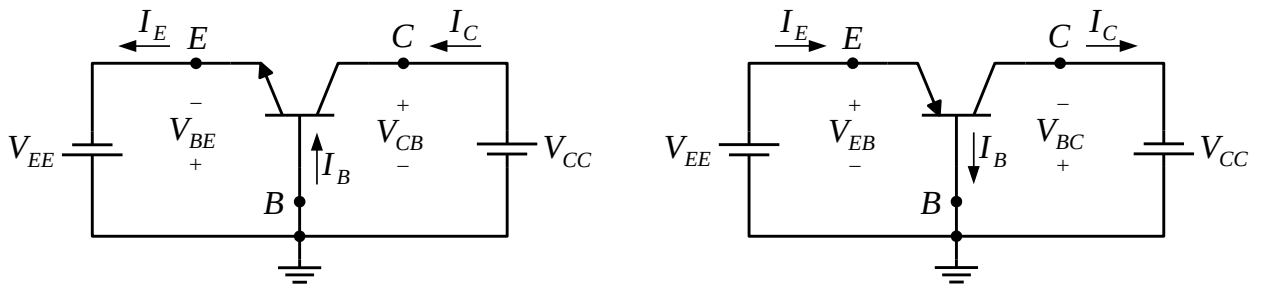


Fig.3-4.Common base (CB) configuration.

In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called **alpha** (α_{dc}) and defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E} \quad [3.3]$$

Where I_C and I_E are the levels of current at the point of operation and $\alpha_{dc} \approx 1$, or for practical devices: $0.900 \leq \alpha_{dc} \leq 0.998$.

Since alpha is defined solely for the majority carriers and from Fig. 3-5, Eq. [3.2] becomes

$$I_C = \alpha I_E + I_{CBO} \quad [3.4]$$

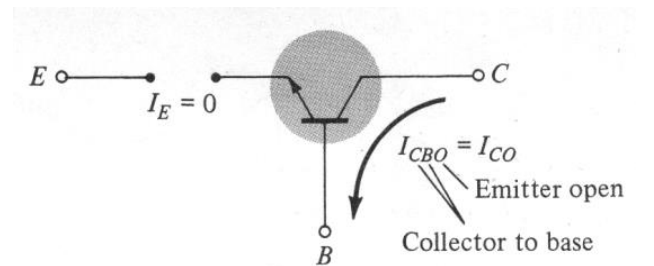


Fig. 3-5

The input (emitter) characteristics for a CB configuration are a plot of the emitter (input) current (I_E) versus the base-to-emitter (input) voltage (V_{BE}) for a range of values of the collector-to-base (output) voltage (V_{CB}) as shown in Fig. 3-6. Since, the exact shape of this I_E - V_{BE} curve will depend on the reverse-biasing output voltage, V_{CB} . The reason for this dependency is that the greater the value of V_{CB} , the more readily minority carriers in the base are swept through the C-B junction. The increase in emitter-to-collector current resulting from an increase in V_{CB} means the emitter current will be greater for a given value of base-to-emitter voltage (V_{BE}).

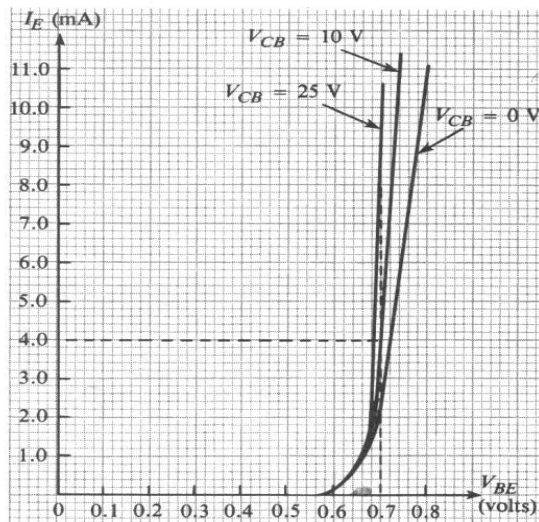


Fig. 3-6. I_E - V_{BE} curve

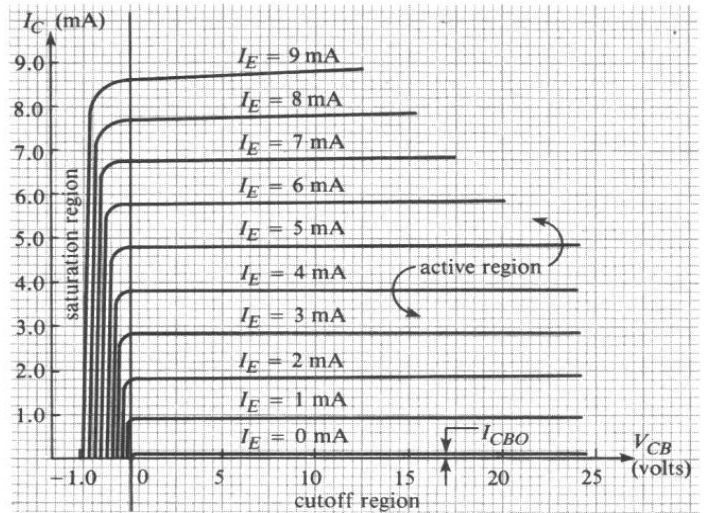


Fig. 3-7. I_C - V_{CB} curve

The output (collector) characteristics for CB configuration will be a plot of the collector (output) current (I_C) versus collector-to-base (output) voltage (V_{CB}) for a range of values of emitter (input) current (I_E) as shown in Fig. 3-7. The collector characteristics have three basic region of interest, as indicated in Fig. 3-7, the active, cutoff, and saturation regions.

- ◀ Active region: $V_{CB} > 0$ and $I_C = \alpha I_E$.
- ◀ Cutoff region: $I_E = 0$ and $I_C = I_{CBO}$.
- ◀ Saturation region: $V_{CB} < 0$ and $I_{C(sat.)} \approx I_{E(sat.)}$.

For ac situations where the point of operation moves on the characteristic curve, an ac alpha (α_{ac}) is defined by:

$$\alpha_{ac} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB} = \text{const.}}$$

[3.5]

The ac alpha is formally called the **common-base, short-circuit, amplification factor**, and for most situations the magnitudes of α_{ac} and α_{dc} are quite close, permitting the use of the magnitude of one for other.

Fig. 3-8 shows how the common-base output characteristics appear when the effects of breakdown are included. Note the sudden upward swing of each curve at a large value of V_{CB} . The collector-to-base breakdown voltage when $I_E = 0$ (emitter open) is designated BV_{CBO} .

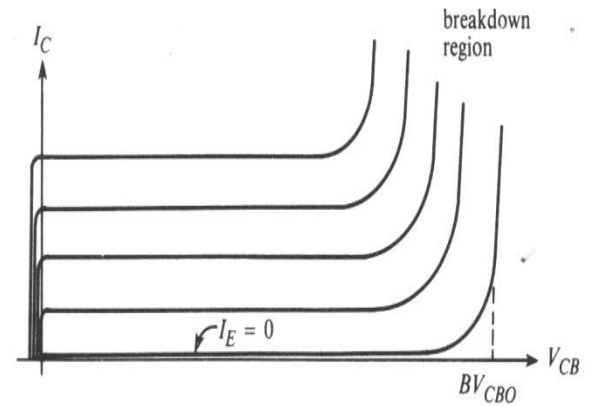


Fig. 3-8. CB output characteristics

Transistor Amplification Action:

The basic voltage-amplifying action of the CB configuration can now be described using the circuit of Fig. 3-9. The dc biasing does not appear in the figure since our interest will be limited to the ac response. For the CB configuration, the input resistance between the emitter and the base of a transistor will typically vary from 10 to 100 Ω , while the output resistance may vary from 100 k Ω to 1 M Ω . The difference in resistance is due to the forward-biased junction at the input (base to emitter) and the reverse-biased junction at the output (base to collector). Using effective values and a common value of 20 Ω for the input resistance, we find that

$$I_i = V_i / R_i = 200\text{mV} / 20\Omega = 10\text{mA}.$$

If we assume for the moment that

$$\alpha_{ac} = 1 \quad (I_c = I_e),$$

$$I_L = I_i = 10\text{mA}$$

$$\text{and } V_L = I_L R = (10\text{mA})(5\text{k}\Omega) = 50\text{V}.$$

The voltage amplification is

$$A_v = V_L / V_i = 50\text{V} / 200\text{mV} = 250.$$

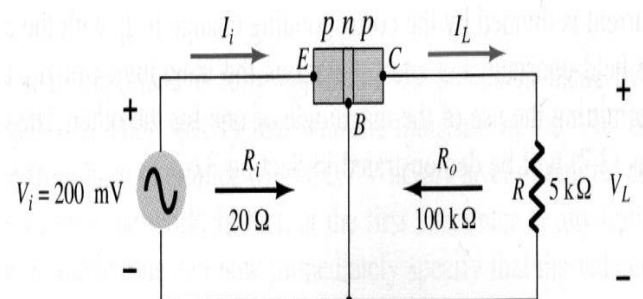


Fig.3-9.Amplifying action of
CB configuration

Typical values of voltage amplification for the common-base configuration vary from 50 to 300. The current amplification (I_C/I_E) is always less than 1 for the CB configuration. This latter characteristic should be obvious since $I_C = \alpha I_E$ and α is always less than 1.

The basic amplifying action was produced by *transferring* a current I from a low-to a high-*resistance* circuit. The combination of the two terms in italics results in the label transistor; that is, *transfer* + *resistor* $\rightarrow$ *transistor*.

Common-Emitter (CE) Configuration:

The common-emitter configuration with npn and pnp transistors are indicated in Fig.(3-10). The external voltage source V_{BB} is used to forward bias the E-B junction and the external voltage source V_{CC} is used to reverse bias C-B junction. The magnitude of V_{CC} must be greater than V_{BB} to ensure the C-B junction remains reverse biased, since, as can be seen in the Fig. 3-10, $V_{CB} = V_{CC} - V_{BB}$.

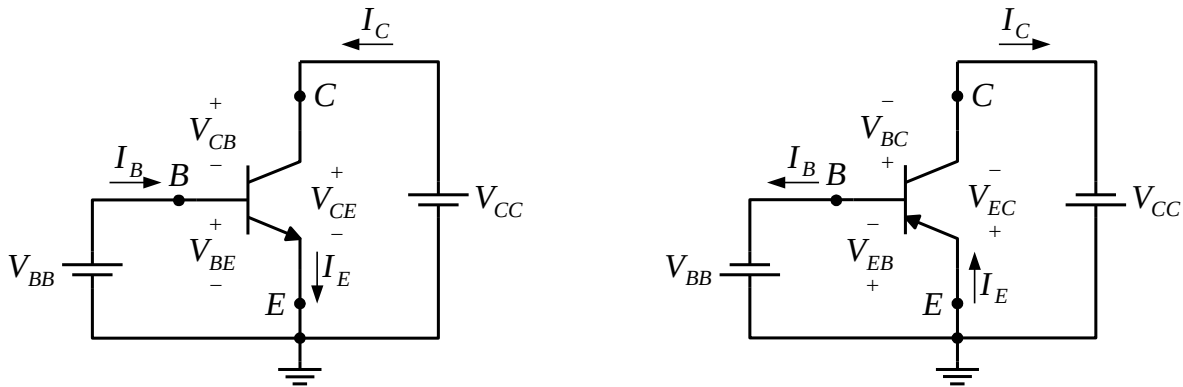


Fig. 3-10. CE configuration

From Eqs. [3.1] and [3.4], we obtain:

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

Rearranging yields :

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha} \quad [3.6]$$

From Fig. 3-11, Eq. [3.6] becomes:

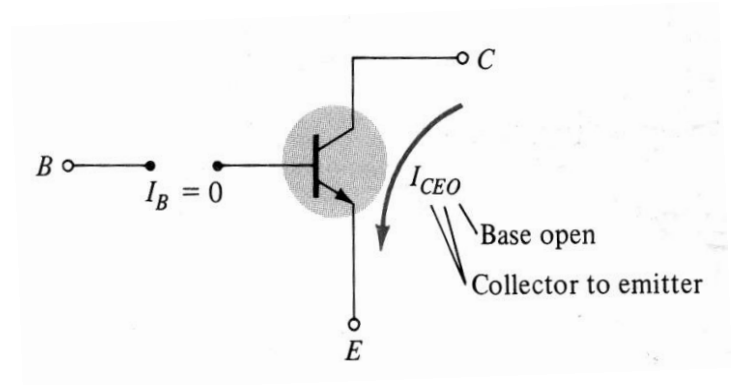


Fig. 3-11.

$$\boxed{I_{CEO} = \frac{I_{CBO}}{1 - \alpha} \Big|_{I_B=0}} \quad [3.7]$$

In the dc mode the levels of I_C and I_B are related by a quantity called **beta** (β_{dc}) and defined by the following equation:

$$\boxed{\beta_{dc} = \frac{I_C}{I_B}} \quad [3.8]$$

Where I_C and I_B are the levels of current at the point of operation. For practical devices the levels of β_{dc} typically ranges from about 50 to over 500, with most in the mid range. On specification sheets β_{dc} is usually included as **h_{FE}** with h derived from an ac hybrid equivalent circuit.

For ac situation an ac beta (β_{ac}) has been defined as follows:

$$\boxed{\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \Big|_{V_{CE}=const.}} \quad [3.9]$$

The formal name for β_{ac} is **common-emitter, forward-current, amplification factor** and on specification sheets β_{ac} is usually included as **h_{fe}** .

A relationship can be developed between β and α using the basic relationships introduced thus far. Using $\beta = I_C / I_B$ we have $I_B = I_C / \beta$, and from $\alpha = I_C / I_E$ we have $I_E = I_C / \alpha$. Substituting into $I_E = I_C + I_B$ we have $I_C / \alpha = I_C + I_C / \beta$ and dividing both sides of the equation by I_C will result in $1/\alpha = 1 + 1/\beta$ or $\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$ so that :

$$\boxed{\alpha = \frac{\beta}{\beta + 1} \quad \text{or} \quad \beta = \frac{\alpha}{1 - \alpha}} \quad [3.10]$$

In addition, recall that $I_{CEO} = I_{CBO} / (1 - \alpha)$ but using an equivalence of $1/(1 - \alpha) = \beta + 1$ derived from the above, we find that $I_{CEO} = (\beta + 1)I_{CBO}$ or

$$\boxed{I_{CEO} \cong \beta I_{CBO}} \quad [3.11]$$

Beta is particularly important parameter because it provides a direct link between current levels of the input and output circuits for CE configuration. That is :

$$I_C = \beta I_B + I_{CEO} \approx \beta I_B \quad [3.12]$$

and since $I_E = I_C + I_B = \beta I_B + I_B$ we have :

$$I_E = (\beta + 1)I_B \quad [3.13]$$

The input (base) characteristics for the CE configuration are a plot of the base (input) current (I_B) versus the base-to-emitter (input) voltage (V_{BE}) for a range of values of collector-to-emitter (output) voltage (V_{CE}) as shown in Fig. 3-12. Note that I_B increases as V_{CE} decreases, for a fixed value of V_{BE} . A large value of V_{CE} results in a large reverse bias of the C-B junction, which widens the depletion region and makes the base smaller. When the base is smaller, there are fewer recombinations of injected minority carriers and there is a corresponding reduction in base current (I_B).

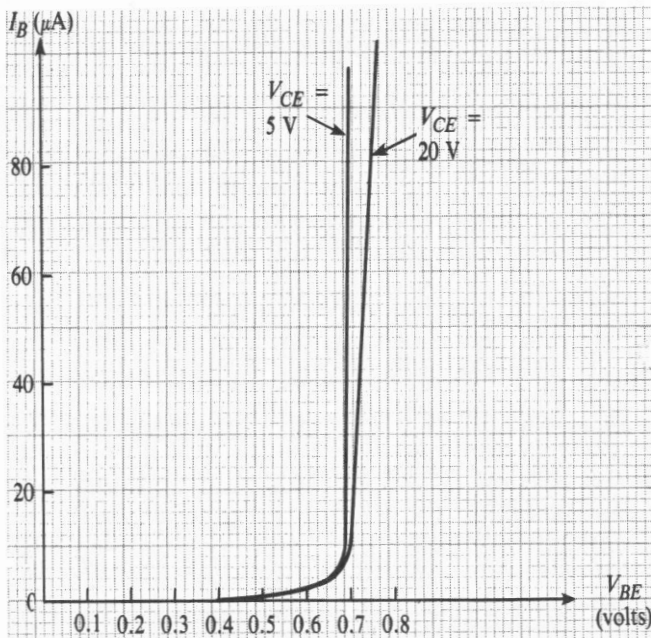


Fig. 3-12. I_B versus V_{BE}

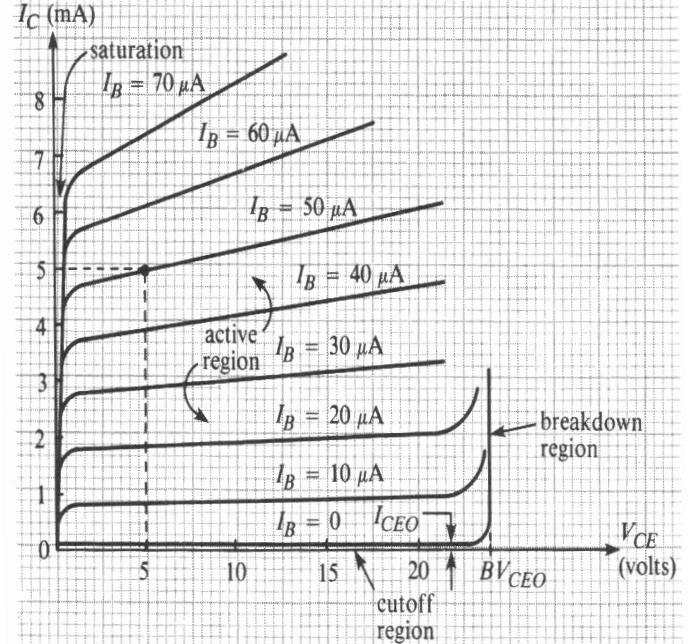


Fig. 3-13. Output characteristics for CE

The output (collector) characteristics for CE configuration are a plot of the collector (output) current (I_C) versus collector-to-emitter (output) voltage (V_{CE}) for a range of values of base (input) current (I_B) as shown in Fig. 3-13. The collector

characteristics have three basic region of interest, as indicated in Fig. 3-13, the active, cutoff, and saturation regions.

- ◀ Active region: $I_B > 0$ and $I_C = \beta I_B$.
- ◀ Cutoff region: $I_B = 0$ and $I_C = I_{CEO}$.
- ◀ Saturation region: $V_{CE} \approx 0$ and $I_{B(sat.)} = I_{C(sat.)} / \beta$.

Common-Collector (CC) Configuration:

The third and final transistor configuration is the common-collector configuration, shown in Fig. 3-14 with NPN and PNP transistors. The CC configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that which is true of the common-base and common-emitter configurations.

From a design viewpoint, there is no need for a set of common-collector characteristics to choose the circuit parameters. The circuit can be designed using the common-emitter characteristics. For all practical purposes, the output characteristics of the CC configuration are the same as for the CE configuration. For the CC configuration the output characteristics are a plot of emitter (output) current (I_E) versus collector-to-emitter (output) voltage (V_{CE}), for a range of values of base (input) current (I_B). The output current, therefore, is the same for both the common-emitter and common-collector characteristics. There is an almost unnoticeable change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics (since $\alpha \cong 1$, $I_E \approx I_C$).

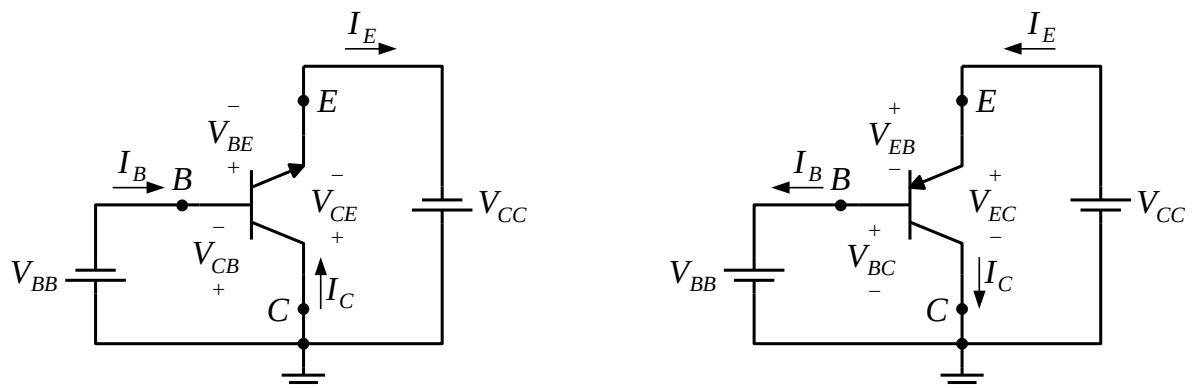


Fig. 3-14. CC configuration

3-2: DC analysis, Load line and Q-point:

Load-Line Analysis - Input Side

Figure (3-15) shows the input characteristic of the transistor with input load line. Remember that the base-emitter is a *diode* and the *Thevenin resistance* is constant and *voltage* varies with time. Thus, the load line has constant slope ($-1/R_B$), and *moves with time*.

From Figure (3-15), It can be noted that:

1. The load line shown for $V_{in} = 0$. When $V_{in} = 0$, only dc remains in the circuit. This I_B , V_{BE} operating point is called the *quiescent point* (*Q-point*) is given special notation:

$$I_{BQ}, V_{BEQ}$$

2. Maximum excursion of load line with V_{in} is shown in Figure (3-15)
3. Minimum excursion of load line with V_{in} is shown in Figure (3-15). Thus, as V_{in} varies through its cycle, base current varies from i_{Bmax} to i_{Bmin} . The base-emitter voltage varies also, from V_{BEmax} to V_{BEmin} .

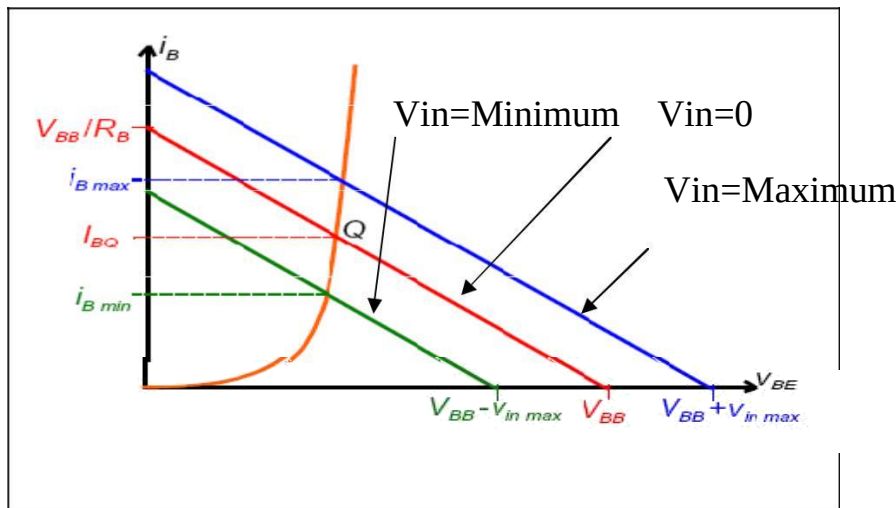


Figure (3-15): Load line on the input characteristics

Load-Line Analysis - Output Side:

Returning to the circuit, observe that V_{CC} and R_C form a Thevenin equivalent, with output variables I_C and V_{CE} . Thus we can plot this load line on the transistor *output characteristics*, (fig. 3-16) because neither V_{CC} nor R_C are time-varying, this load line is fixed.

1. The collector-emitter operating point is given by the intersection of the load line and the appropriate base current curve. When $V_{in} = 0$, $I_B = I_{BQ}$, and the quiescent point is I_{CQ} , V_{CEQ} . At $V_{in\ max}$, $I_B = I_{B\ max}$, and the operating point is $I_{C\ max}$, $V_{CE\ min}$. At $V_{in\ min}$, $I_B = I_{B\ min}$, and the operating point is $I_{C\ min}$, $V_{CE\ max}$.
2. If the total change in V_{CE} is greater than total change in V_{in} , we have an amplifier

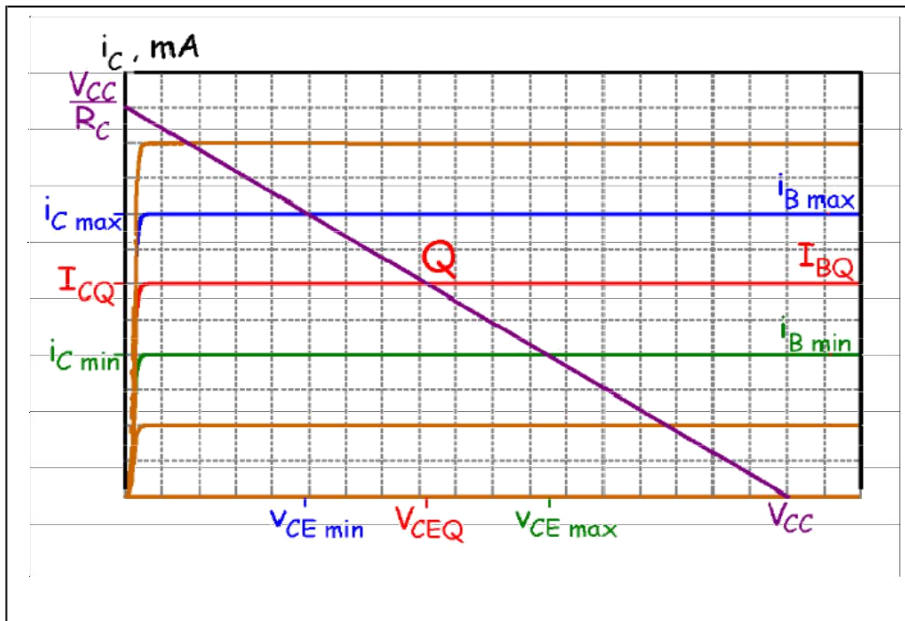


Figure (3-16): DC load line on the output characteristics

Q-point:

For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated Q-point). By definition, *quiescent* means quiet, still, inactive. Figure (3-17) shows a general output device characteristic with four operating points indicated (A,B,C,D). The biasing circuit can be designed to set the device operation at any of these points or others within the *active region*. The maximum ratings are indicated on the characteristics of Fig.(3-17) by a horizontal line for the maximum collector current $I_{C\ max}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE\ max}$. The maximum power constraint is defined by the curve $P_{C\ max}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by I_{B0} , and the *saturation region*, defined by $V_{CE} = V_{CE\ sat}$.

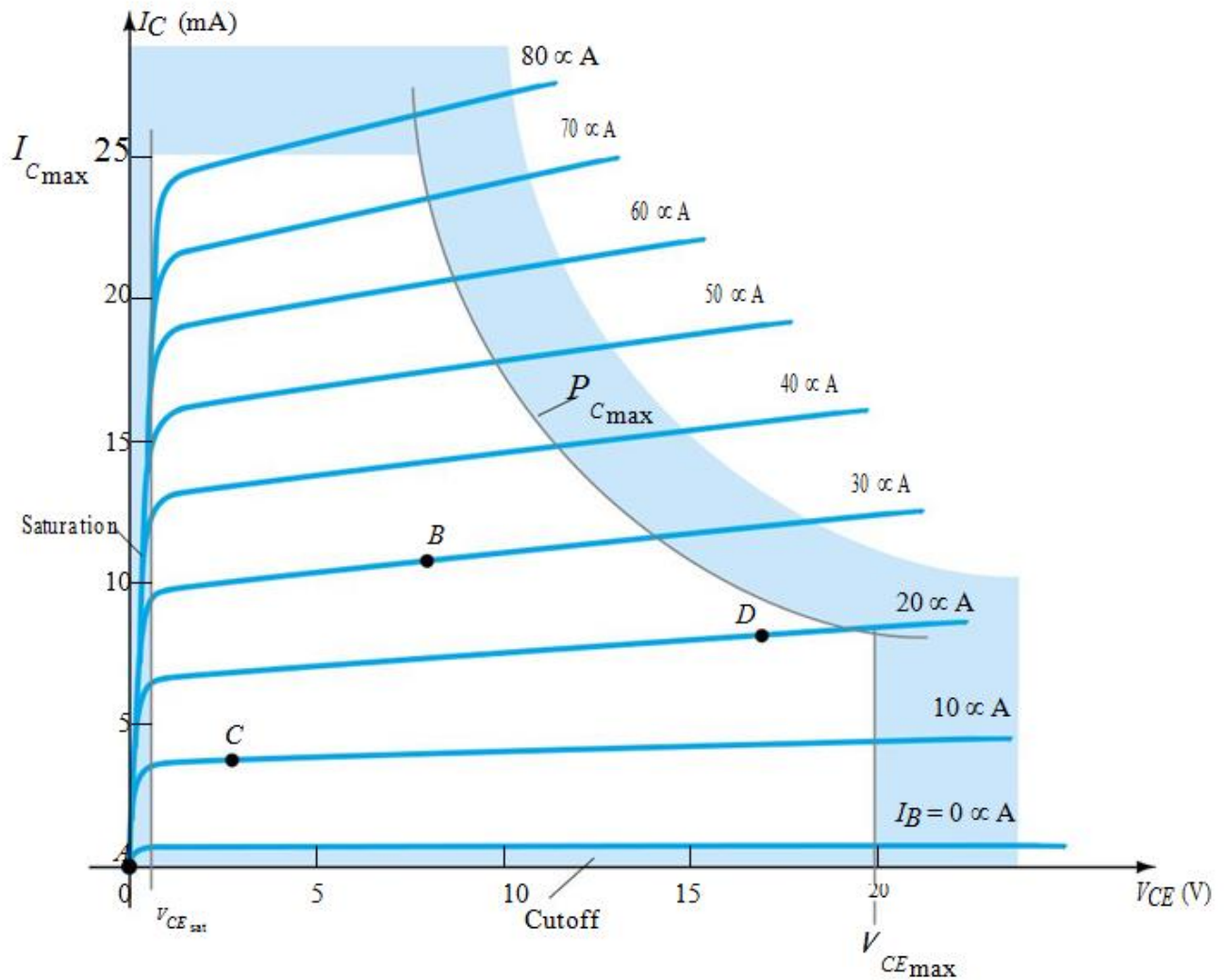


Figure (3-17). Various operating points within the limits of operation of a transistor

3-3: BJT Transistor AC Equivalent Circuits, h- parameters and re-model:

Hybrid Parameters

Every *linear circuit having input and output terminals can be analysed by four parameters (one measured in ohm, one in mho and two dimensionless) called hybrid or h Parameters.

Hybrid means “mixed”. Since these parameters have mixed dimensions, they are called hybrid parameters. Consider a linear circuit shown in Fig. 3.18. This circuit has input voltage and current labelled v_1 and i_1 . This circuit also has output voltage and current labelled v_2 and i_2 . Note that both input and output currents (i_1 and i_2) are assumed to flow *into* the box ; input and output voltages (v_1 and v_2) are assumed

positive from the upper to the lower terminals. These are standard conventions and do not necessarily correspond to the actual directions and polarities. When we analyse circuits in which the voltages are of opposite polarity or where the currents flow out of the box, we simply treat these voltages and currents as negative quantities.

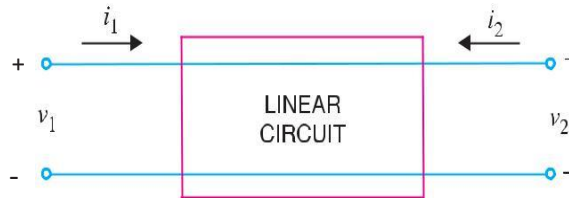


Figure (3-18). h-parameters analysis circuit

It can be proved by advanced circuit theory that voltages and currents in Fig. 3.18 can be related by the following sets of equations :

$$v_1 = h_{11} i_1 + h_{12} v_2 \quad \dots(i)$$

$$i_2 = h_{21} i_1 + h_{22} v_2 \quad \dots(ii)$$

In these equations, the h_s are fixed constants for a given circuit and are called

h - parameters. Once these parameters are known, we can use equations (i) and (ii) to find the voltages and currents in the circuit. If we look at eq.(i), it is clear that h_{11} has the dimension of ohm and h_{12} is dimension-less. Similarly, from eq. (ii), h_{21} is dimensionless and h_{22} has the dimension of mho. The following points may be noted about h parameters :

- (i) Every linear circuit has four h parameters ; one having dimension of ohm, one having dimension of mho and two dimensionless.
- (ii) The h parameters of a given circuit are constant. If we change the circuit, h parameters would also change.
- (iii) Suppose that in a particular linear circuit, voltages and currents are related as under:

$$v_1 = 10i_1 + 6v_2$$

$$i_2 = 4i_1 + 3v_2$$

*A linear circuit is one in which resistances, inductances and capacitances remain fixed when voltage across them changes.

The two parts on the R.H.S. (R**ight **H**and **S**ide) of eq. (i) must have the unit of voltage. Since current (amperes) must be multiplied by resistance (ohms) to get voltage (volts), h_{11} should have the dimension of resistance *i.e.* ohms.

Summary of the BJT current-voltage relationships in the active mode

- ❑ The terminal currents for a BJT in active mode solely depend on the junction voltage v_{BE}
- ❑ The ratios of the terminal currents for a BJT in active mode are constant
- ❑ The current directions for *nnp* and *pnp* transistors are opposite

<i>nnp</i> transistor	<i>pnp</i> transistor	
$i_C = I_S e^{v_{BE}/V_T}$	$i_C = I_S e^{v_{EB}/V_T}$	$i_E = i_C + i_B$
$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T}$	$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{EB}/V_T}$	$\alpha = \frac{\beta}{\beta + 1}$
$i_E = \frac{i_C}{\alpha} = \frac{I_S}{\alpha} e^{v_{BE}/V_T}$	$i_E = \frac{i_C}{\alpha} = \frac{I_S}{\alpha} e^{v_{EB}/V_T}$	$\beta = \frac{\alpha}{1 - \alpha}$

3-4: Applications: Transistor Amplifier:

Examples :

EXAMPLE 3.1:

- (a) Using the characteristics of Fig. 3.19, determine the resulting collector current if $I_E = 3 \text{ mA}$ and $V_{CB} = 10 \text{ V}$.
- (b) Using the characteristics of Fig. 3.19, determine the resulting collector current if I_E remains at 3 mA but V_{CB} is reduced to 2 V .
- (c) Using the characteristics of Figs. 3.20 and 3.19, determine V_{BE} if $I_C = 4 \text{ mA}$ and $V_{CB} = 20 \text{ V}$.

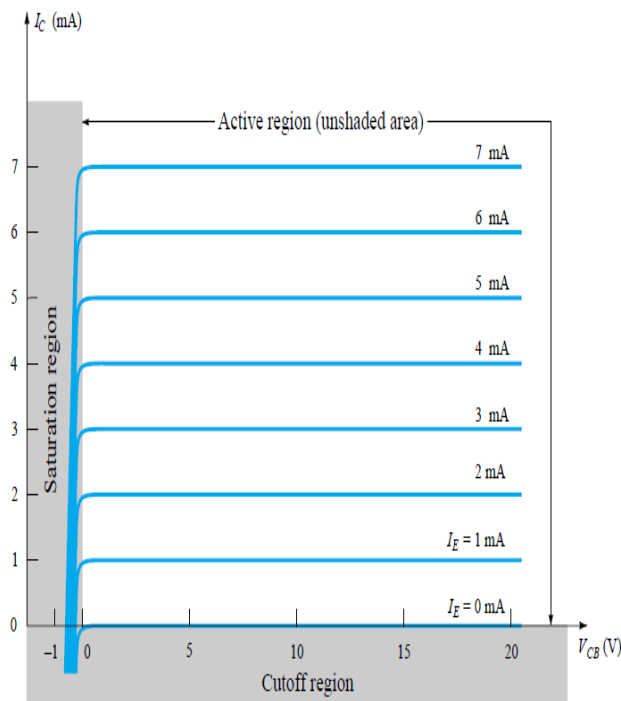


Fig.(3-19). Output or collector characteristics for a common-base transistor amplifier.

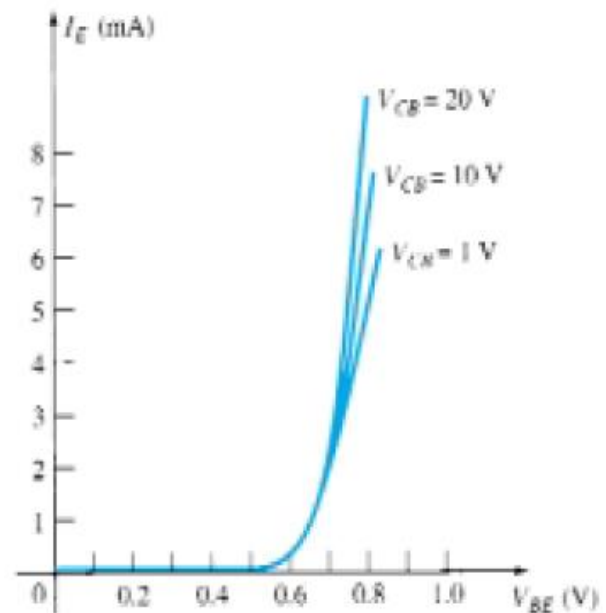


Fig.(3-20). Input or Driving point characteristics for common-base silicon transistor amplifier

Solution

- (a) The characteristics clearly indicate that $I_C \cong I_E = 3 \text{ mA}$.
- (b) The effect of changing V_{CB} is negligible and I_C continues to be 3 mA .
- (c) From Fig. 3.19, $I_E \cong I_C = 4 \text{ mA}$. On Fig. 3.20 the resulting level of V_{BE} is about **0.74 V**.

Example 3 -2 :

Repeat part (c) of Example -1 above using the characteristics of Figs. 3.19 and 3.21.

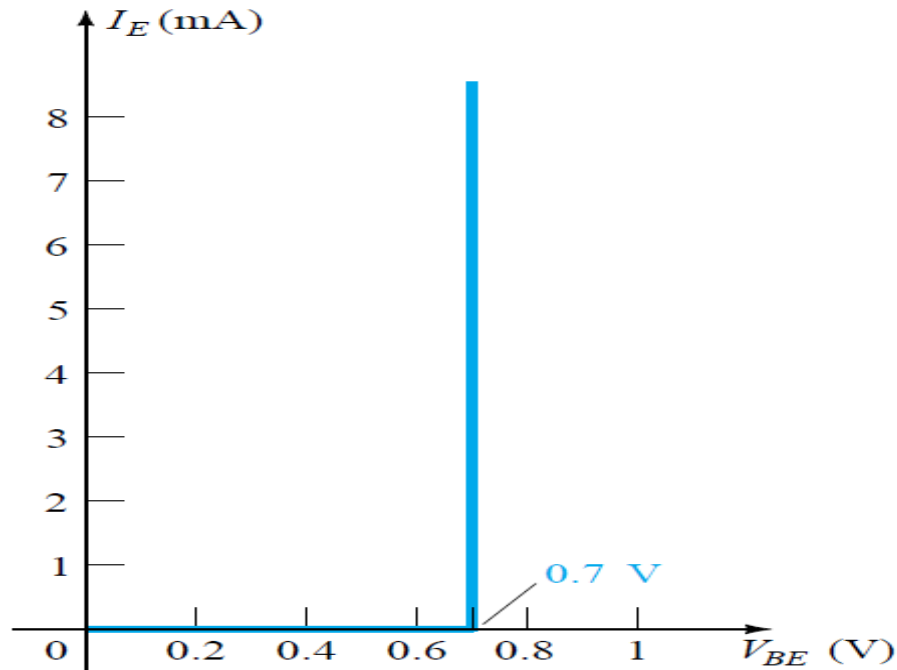


Fig.(3-21).

Solution:

Again from Fig. 3.19, $I_E \cong I_C = 4$ mA. However, on Fig. 3.21, V_{BE} is **0.7 V** for any level of emitter current.

Example -3 :

Determine the voltage gain A_v for the following common – base circuit.

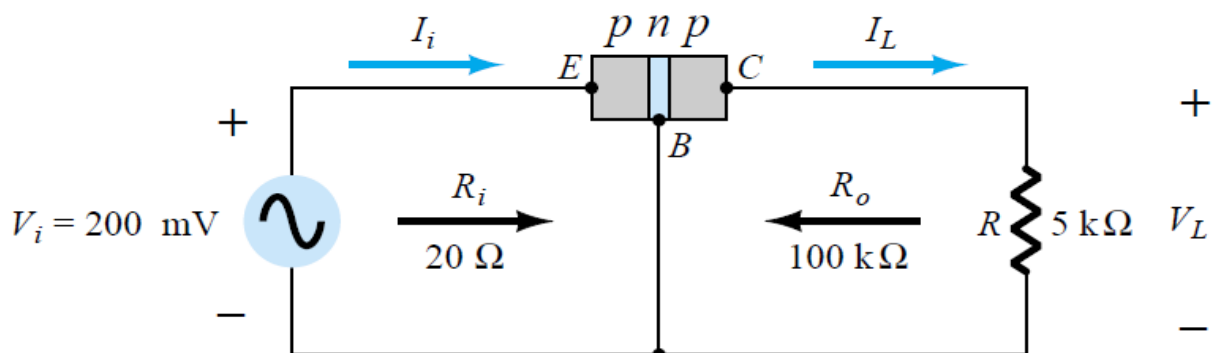


Fig.(3-22). Basic Amplification action of the common –base configuration.

Solution:

$$I_i = \frac{V_i}{R_i} = \frac{200 \text{ mV}}{20 \text{ } \Omega} = \mathbf{10 \text{ mA}}$$

If we assume for the moment that $\alpha_{ac} = 1$ ($I_c = I_e$),

$$I_L = I_i = 10 \text{ mA}$$

and

$$\begin{aligned} V_L &= I_L R \\ &= (10 \text{ mA})(5 \text{ k}\Omega) \\ &= \mathbf{50 \text{ V}} \end{aligned}$$

The voltage amplification is

$$A_v = \frac{V_L}{V_i} = \frac{50 \text{ V}}{200 \text{ mV}} = \mathbf{250}$$

Typical values of voltage amplification for the common-base configuration vary from 50 to 300. The current amplification (I_C/I_E) is always less than 1 for the common-base configuration. This latter characteristic should be obvious since $I_C = \alpha I_E$ and α is always less than 1.

Review Problems:

- Q.1.** Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.22 if $V_i = 500$ mV and $R = 1 \text{ k}\Omega$. (The other circuit values remain the same.)
- Q.2.** Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.22 if the source has an internal resistance of $100 \text{ } \Omega$ in series with V_i .

Chapter – 4

FET Transistors

4-1: FET Transistor :

FET TYPES: There are two types of FET (**F**ield **E**ffect **T**ransistor) transistors:

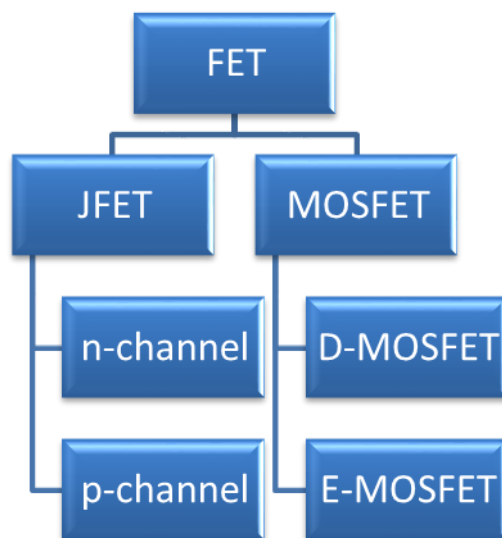


Fig. (4-1).Types of FET Transistors

a). JFET (**J**unction **FET**):

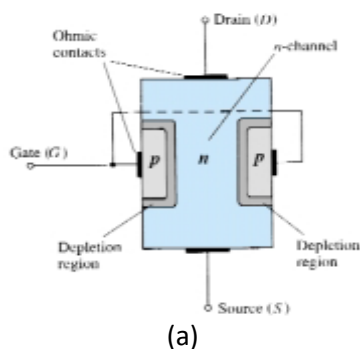
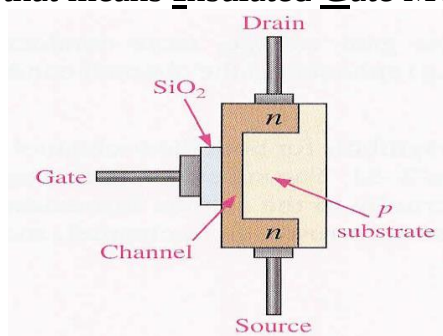
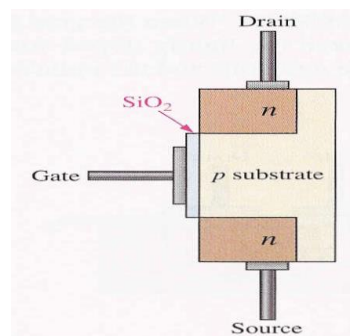


Fig.(4-2). a).JFET transistor , b) Water analogy for the JFET control mechanism

b). MOSFET (Metal Oxide Semiconductor FET) : (or sometimes called IGMOS that means Insulated Gate MOS)



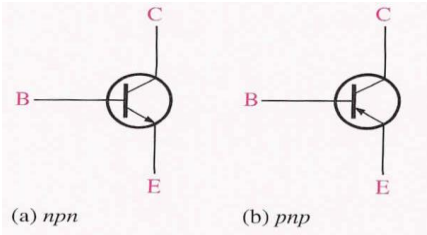
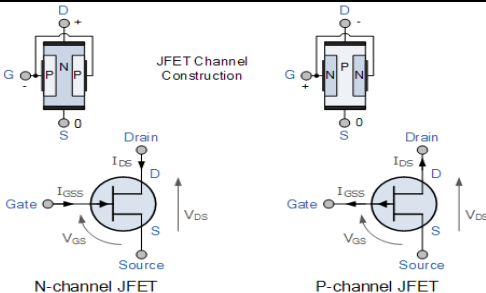
(a). D- MOSFET (n-channel)

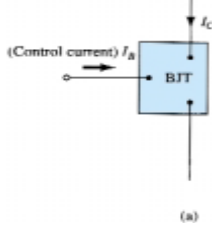
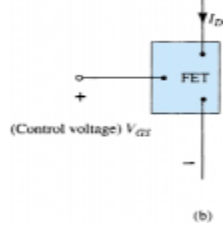


(b). E-MOSFET (n-channel)

Fig.(4-3). a). D (Depletion)- MOSFET transistor , b) E (Enhancement)-MOSFET transistor

Comparison between BJT and FET :

No.	property	BJT	FET												
1.	Symbol	 (a) npn (b) pnp	 N-channel JFET P-channel JFET												
2.	Types	NPN or PNP	JFET : n- channel or p-channel MOSFET: depletion and enhancement channel												
3.	Parameters	<table><tr><td>Base, (B)</td></tr><tr><td>Collector, (C)</td></tr><tr><td>Emitter, (E)</td></tr><tr><td>Base Supply, (V_B)</td></tr><tr><td>Collector Supply, (V_{CC})</td></tr><tr><td>Collector Current, (I_C)</td></tr></table>	Base, (B)	Collector, (C)	Emitter, (E)	Base Supply, (V_B)	Collector Supply, (V_{CC})	Collector Current, (I_C)	<table><tr><td>Gate, (G)</td></tr><tr><td>Drain, (D)</td></tr><tr><td>Source, (S)</td></tr><tr><td>Gate Supply, (V_G)</td></tr><tr><td>Drain Supply, (V_{DD})</td></tr><tr><td>Drain Current, (I_D)</td></tr></table>	Gate, (G)	Drain, (D)	Source, (S)	Gate Supply, (V_G)	Drain Supply, (V_{DD})	Drain Current, (I_D)
Base, (B)															
Collector, (C)															
Emitter, (E)															
Base Supply, (V_B)															
Collector Supply, (V_{CC})															
Collector Current, (I_C)															
Gate, (G)															
Drain, (D)															
Source, (S)															
Gate Supply, (V_G)															
Drain Supply, (V_{DD})															
Drain Current, (I_D)															

4.	Carrier	Bipolar : electrons <u>and</u> holes	Unipolar : either electrons <u>or</u> holes
5.	Control parameter	 (a) Current-controlled amplifier	 (b) Voltage controlled amplifier
6.	Input impedance	<i>low input impedance</i> : about 2KΩ	<i>high input impedance</i> : more than 100MΩ
7.	Current equation	BJT $I_C = \beta I_B$ $I_C \cong I_E$ $V_{BE} \cong 0.7 \text{ V}$ Where : β is constant I_B is control variable	JFET $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$ $I_D = I_S$ $I_G \cong 0 \text{ A}$ Shockley's equation Where : I_{DSS} and V_P is constant V_{GS} is control variable

Advantages of FETs

FETs combine the many advantages of both BJTs and vacuum tubes. Some of their main advantages are :

1. high input impedance,
2. small size,
3. ruggedness,
4. long life,
5. high frequency response,
6. low noise,
7. negative temperature coefficient, hence better thermal stability,
8. high power gain,
9. a high immunity to radiations,
10. no offset voltage when used as a switch (or chopper),
11. square law characteristics.

The only disadvantages are :

1. small gain-bandwidth product,
2. greater susceptibility to damage in handling them.

JFET Structure:

Figure 7–1(a) shows the basic structure of an *n*-channel **JFET** (junction field-effect transistor). Wire leads are connected to each end of the *n*-channel; the **drain** is at the upper end, and the **source** is at the lower end. Two *p*-type regions are diffused in the *n*-type material to form a **channel**, and both *p*-type regions are connected to the **gate** lead. For simplicity, the gate lead is shown connected to only one of the *p* regions. A *p*-channel JFET is shown in Figure 7–1(b).

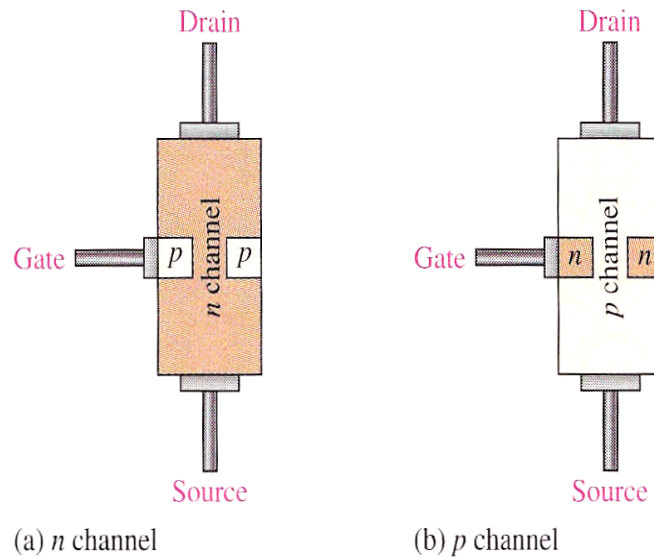


Fig. (4 -4) . Structure of JFET , n-channel and p – channel

Basic Operation

To illustrate the operation of a JFET, Figure 7–2 shows dc bias voltages applied to an n -channel device. V_{DD} provides a drain-to-source voltage and supplies current from drain to source. V_{GG} sets the reverse-bias voltage between the gate and the source, as shown.

The JFET is always operated with the gate-source pn junction reverse-biased. Reverse-biasing of the gate-source junction with a negative gate voltage produces a depletion region along the pn junction, which extends into the n channel and thus increases its resistance by restricting the channel width.

The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, I_D . Figure 7–3 illustrates this concept. The white areas represent the depletion region created by the reverse bias. It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source. We will discuss JFET characteristic curves and some important parameters in Section 7–2.

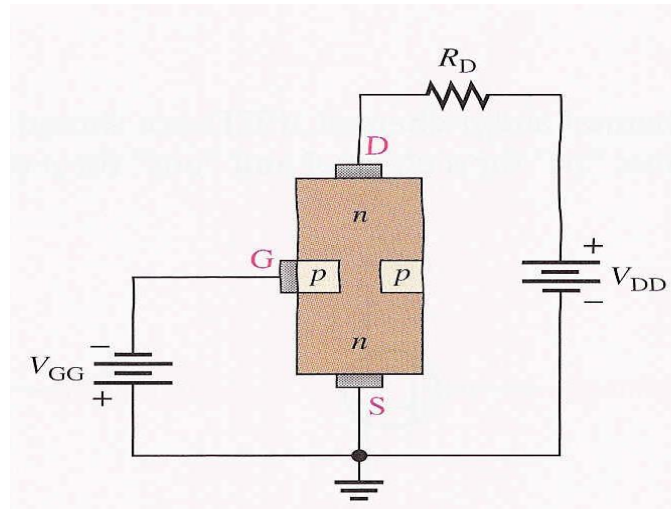


Fig. (4 - 5) . A biased n- channel JFET

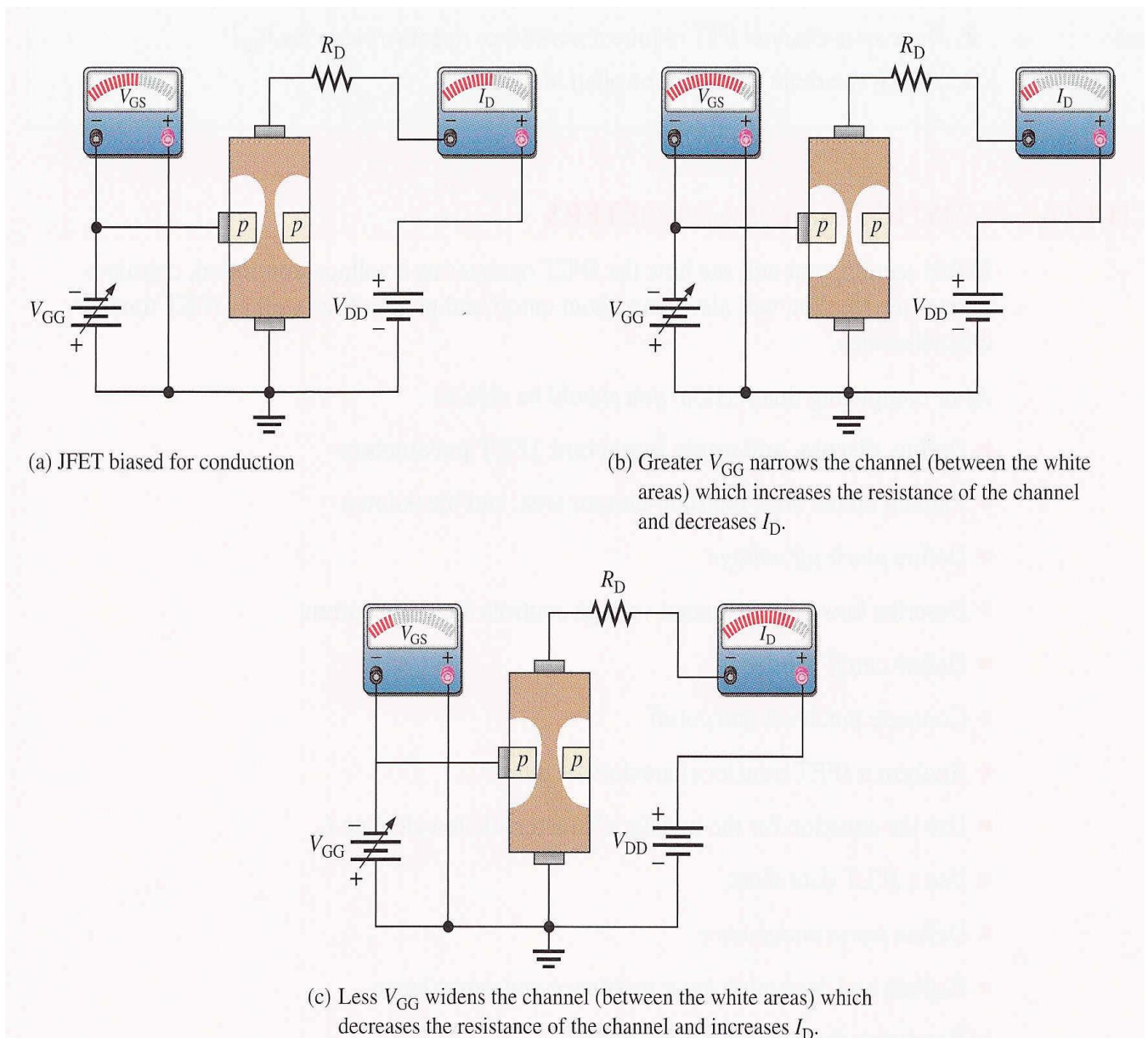


Fig.(4-6). Effect of V_{GS} on channel width , resistance ,and drain current ($V_{GG} = V_{GS}$)

Consider the case when the gate-to-source voltage is zero ($V_{GS} = 0\text{ V}$). This is produced by shorting the gate to the source, as in Figure 7-5(a) where both are grounded. As V_{DD} (and thus V_{DS}) is increased from 0 V, I_D will increase proportionally, as shown in the graph of Figure 7-5(b) between points A and B. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the ohmic area because V_{DS} and I_D are related by Ohm's law.

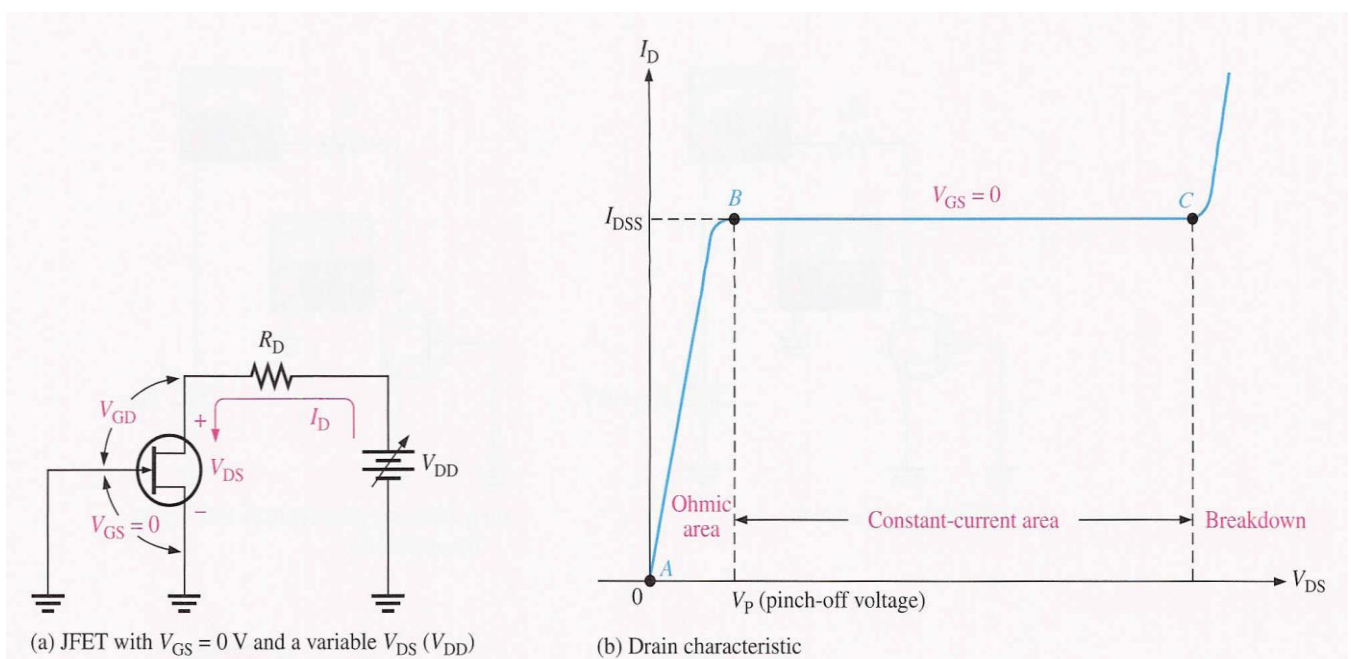


Fig. (4-7).drain characteristics of JFET for $V_{GS}=0$ showing pinch-off

At point *B* in Figure 7–5(b), the curve levels off and I_D becomes essentially constant. As V_{DS} increases from point *B* to point *C*, the reverse-bias voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS} , thus keeping I_D relatively constant.

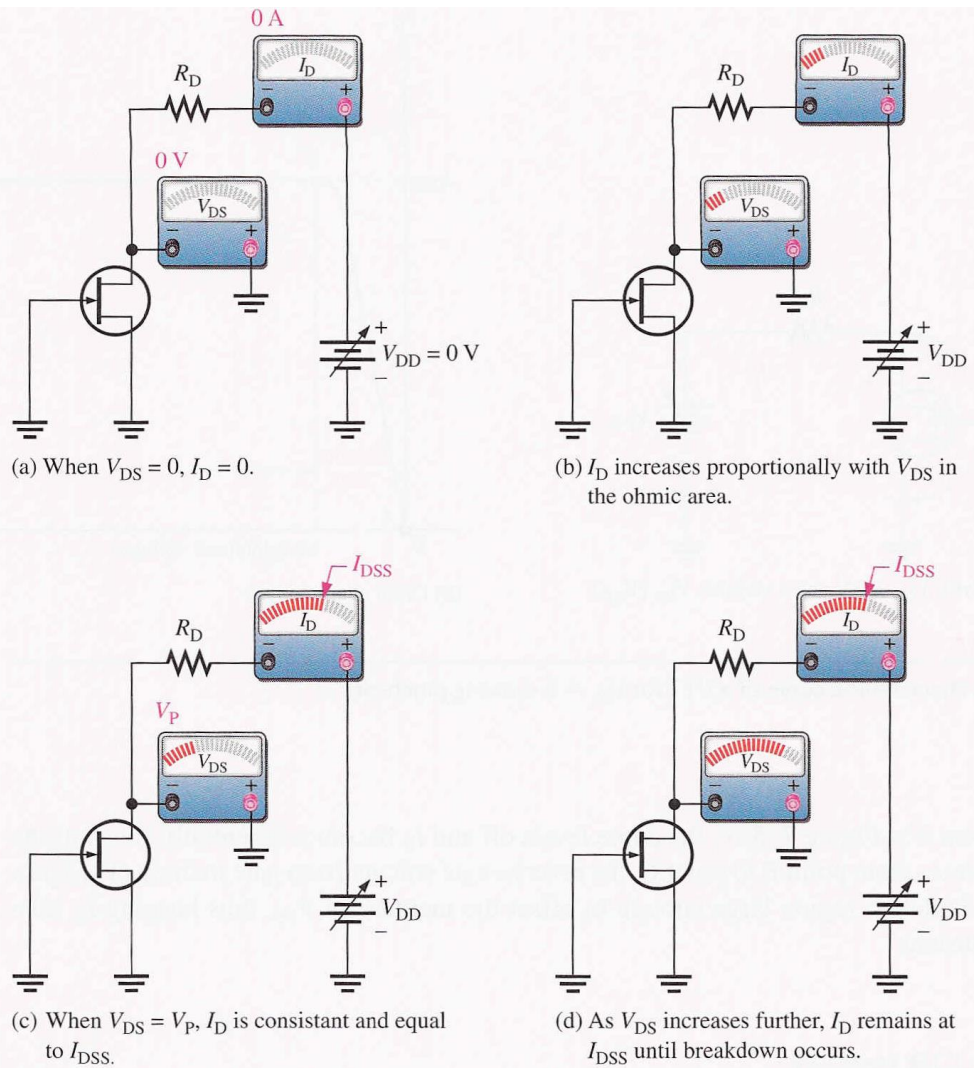
Pinch-Off Voltage

For $V_{GS} = 0$ V, the value of V_{DS} at which I_D becomes essentially constant (point *B* on the curve in Figure 7–5(b)) is the **pinch-off voltage**, V_p . For a given JFET, V_p has a fixed value. As you can see, a continued increase in V_{DS} above the pinch-off voltage produces an almost constant drain current. This value of drain current is I_{DSS} (Drain to Source current with gate Shorted) and is always specified on JFET data sheets. I_{DSS} is the *maximum* drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, $V_{GS} = 0$ V.

As shown in the graph in Figure 7–5(b), **breakdown** occurs at point *C* when I_D begins to increase very rapidly with any further increase in V_{DS} . Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the constant-current area (between points *B* and *C* on the graph). The JFET action that produces the drain characteristic curve to the point of breakdown for $V_{GS} = 0$ V is illustrated in Figure 7–6.

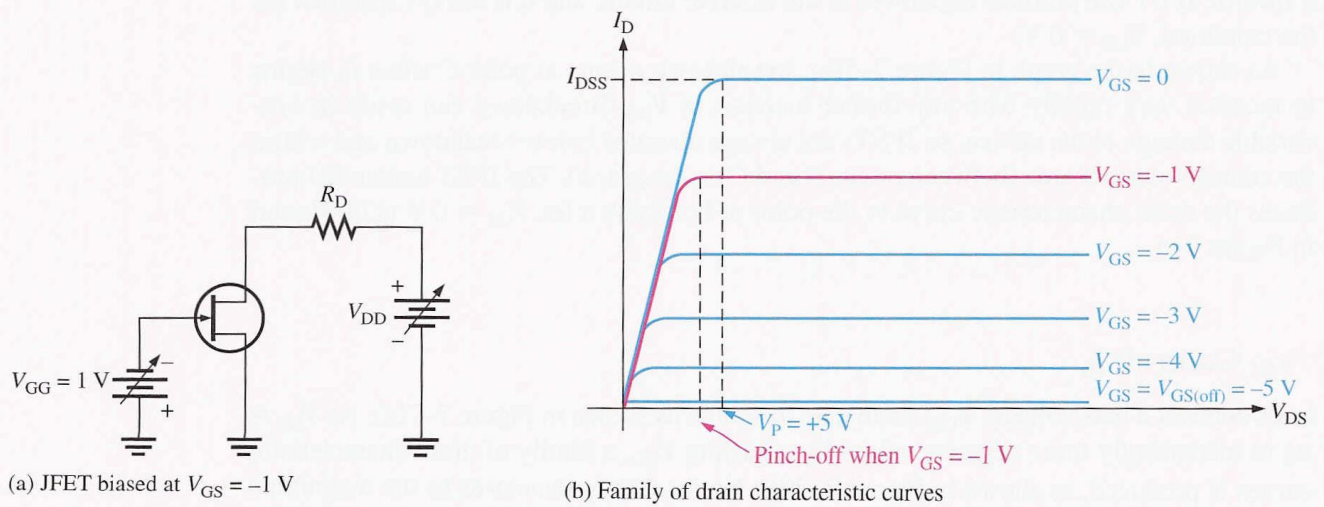
V_{GS} Controls I_D

Let's connect a bias voltage, V_{GG} , from gate to source as shown in Figure 7–7(a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG} , a family of drain characteristic curves is produced, as shown in Figure 7–7(b). Notice that I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in V_{GS} , the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_p . Therefore, the amount of drain current is controlled by V_{GS} , as illustrated in Figure 7–8.



▲ FIGURE 7-6

JFET action that produces the characteristic curve for $V_{GS} = 0$ V.



▲ FIGURE 7-7

Pinch-off occurs at a lower V_{DS} as V_{GS} is increased to more negative values.

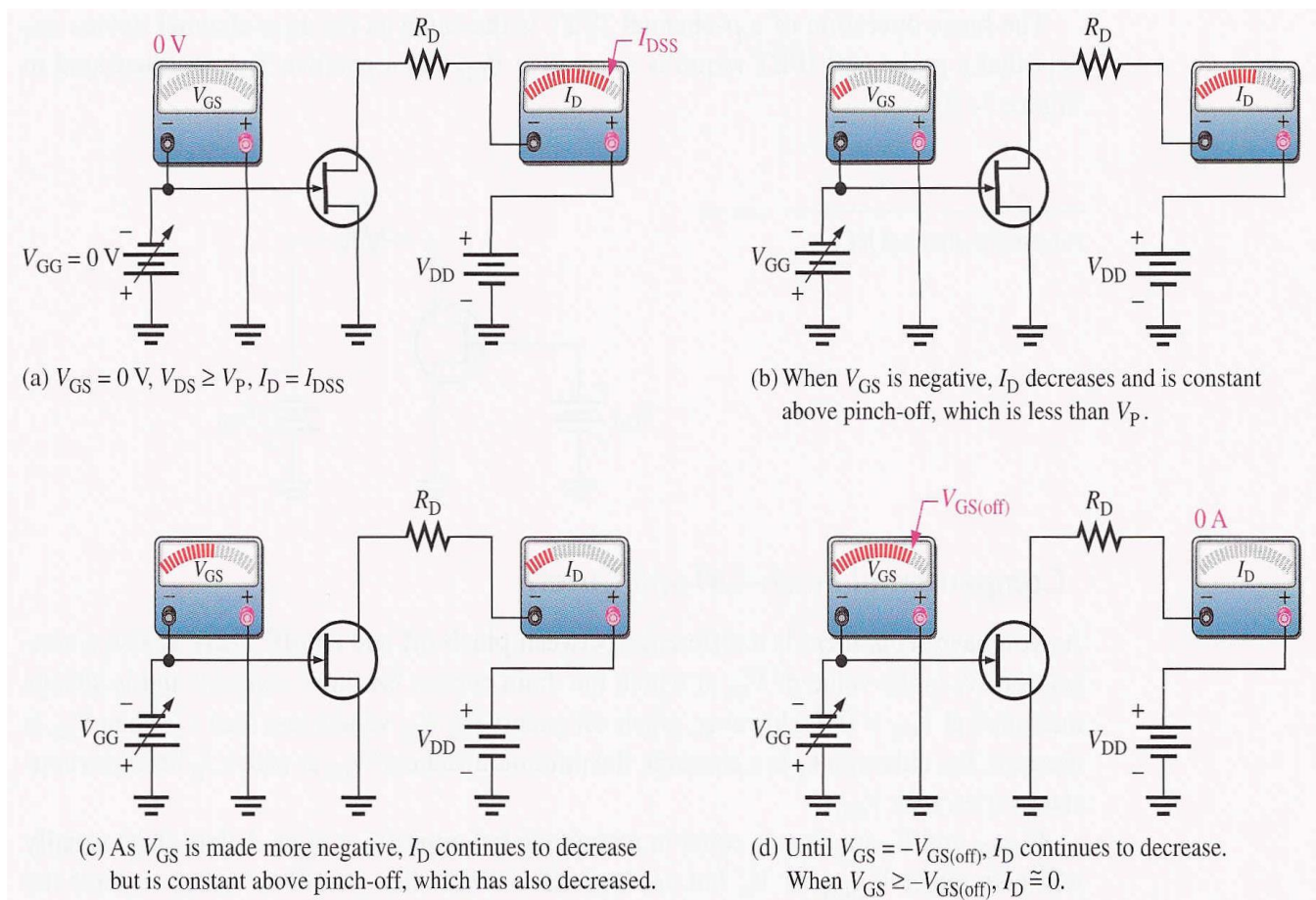


Fig.(4- 10) . V_{GS} controls I_D

Cutoff Voltage

The value of V_{GS} that makes I_D approximately zero is the **cutoff voltage**, $V_{GS(off)}$. The JFET must be operated between $V_{GS} = 0 \text{ V}$ and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

As you have seen, for an n -channel JFET, the more negative V_{GS} is, the smaller I_D becomes in the constant-current area. When V_{GS} has a sufficiently large negative value, I_D is reduced to zero. This cutoff effect is caused by the widening of the depletion region to a point where it completely closes the channel, as shown in Figure 7-9.

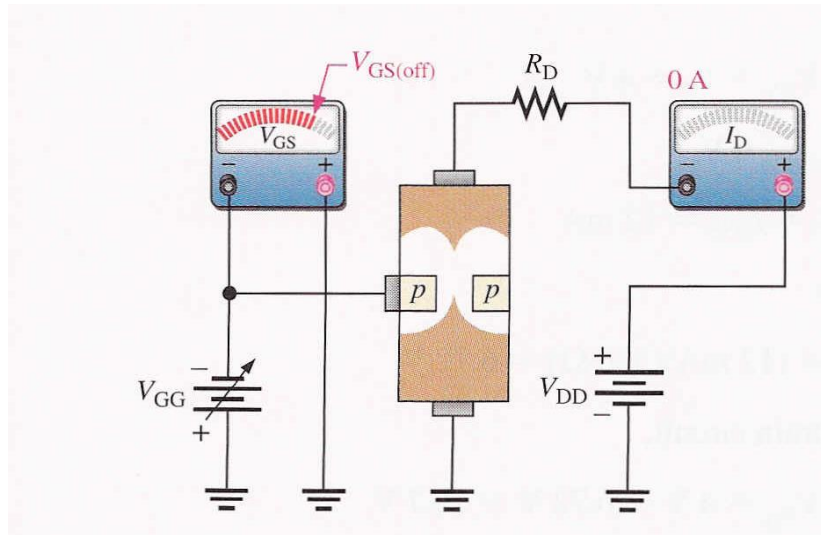
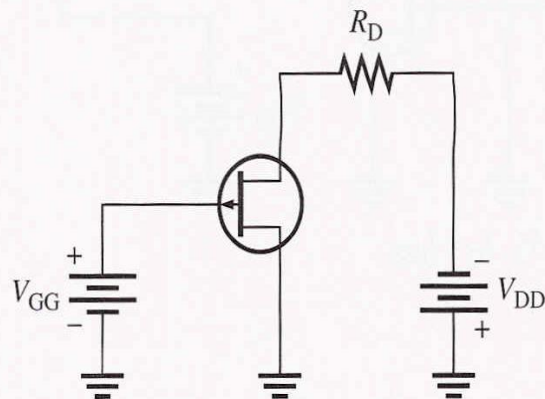


Fig.(4- 11) . JFET at cutoff

The basic operation of a *p*-channel JFET is the same as for an *n*-channel device except that a *p*-channel JFET requires a negative V_{DD} and a positive V_{GS} , as illustrated in Figure 7–10.

► FIGURE 7–10

A biased *p*-channel JFET.



Comparison of Pinch-Off and Cutoff

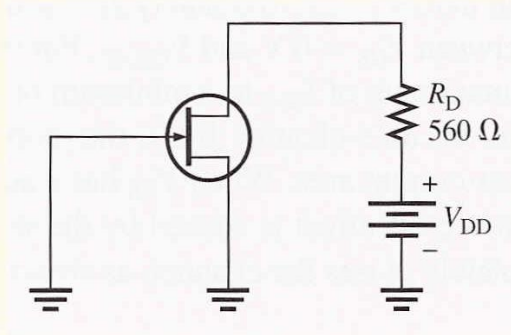
As you have seen, there is a difference between pinch-off and cutoff. There is also a connection. V_P is the value of V_{DS} at which the drain current becomes constant and is always measured at $V_{GS} = 0$ V. However, pinch-off occurs for V_{DS} values less than V_P when V_{GS} is nonzero. So, although V_P is a constant, the minimum value of V_{DS} at which I_D becomes constant varies with V_{GS} .

$V_{GS(off)}$ and V_P are always equal in magnitude but opposite in sign. A data sheet usually will give either $V_{GS(off)}$ or V_P , but not both. However, when you know one, you have the other. For example, if $V_{GS(off)} = -5$ V, then $V_P = +5$ V, as shown in Figure 7–7(b).

Example (4 - 1) :

For the JFET in Figure 7–11, $V_{GS(off)} = -4\text{ V}$ and $I_{DSS} = 12\text{ mA}$. Determine the *minimum* value of V_{DD} required to put the device in the constant-current area of operation.

► **FIGURE 7–11**



Since $V_{GS(off)} = -4\text{ V}$, $V_P = 4\text{ V}$. The minimum value of V_{DS} for the JFET to be in its constant-current area is

$$V_{DS} = V_P = 4\text{ V}$$

In the constant-current area with $V_{GS} = 0\text{ V}$,

$$I_D = I_{DSS} = 12\text{ mA}$$

The drop across the drain resistor is

$$V_{R_D} = I_D R_D = (12\text{ mA})(560\ \Omega) = 6.72\text{ V}$$

Apply Kirchhoff's law around the drain circuit,

$$V_{DD} = V_{DS} + V_{R_D} = 4\text{ V} + 6.72\text{ V} = \mathbf{10.7\text{ V}}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current area.

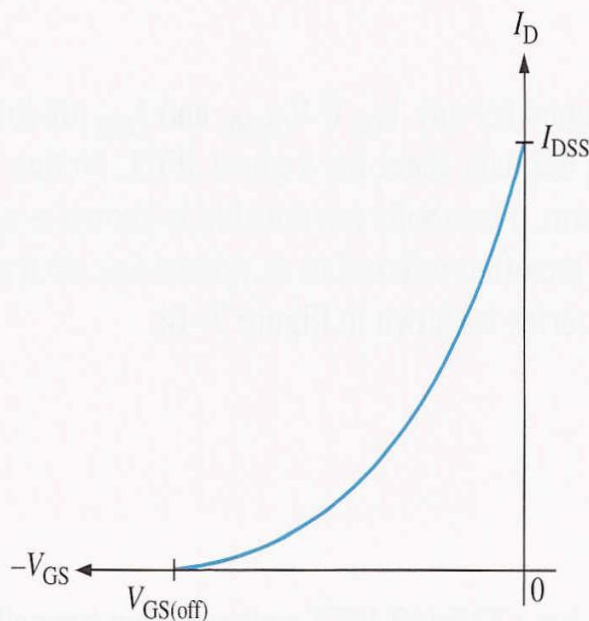
Example (4 - 2) :

A particular *p*-channel JFET has a $V_{GS(off)} = +4\text{ V}$. What is I_D when $V_{GS} = +6\text{ V}$?

The *p*-channel JFET requires a positive gate-to-source voltage. The more positive the voltage, the less the drain current. When $V_{GS} = 4\text{ V}$, $I_D = 0$. Any further increase in V_{GS} keeps the JFET cut off, so I_D remains **0**.

JFET Transfer Characteristic

You have learned that a range of V_{GS} values from zero to $V_{GS(off)}$ controls the amount of drain current. For an n -channel JFET, $V_{GS(off)}$ is negative, and for a p -channel JFET, $V_{GS(off)}$ is positive. Because V_{GS} does control I_D , the relationship between these two quantities is very important. Figure 7–12 is a general transfer characteristic curve that illustrates graphically the relationship between V_{GS} and I_D .



◀ **FIGURE 7-12**

JFET transfer characteristic curve
(n -channel).

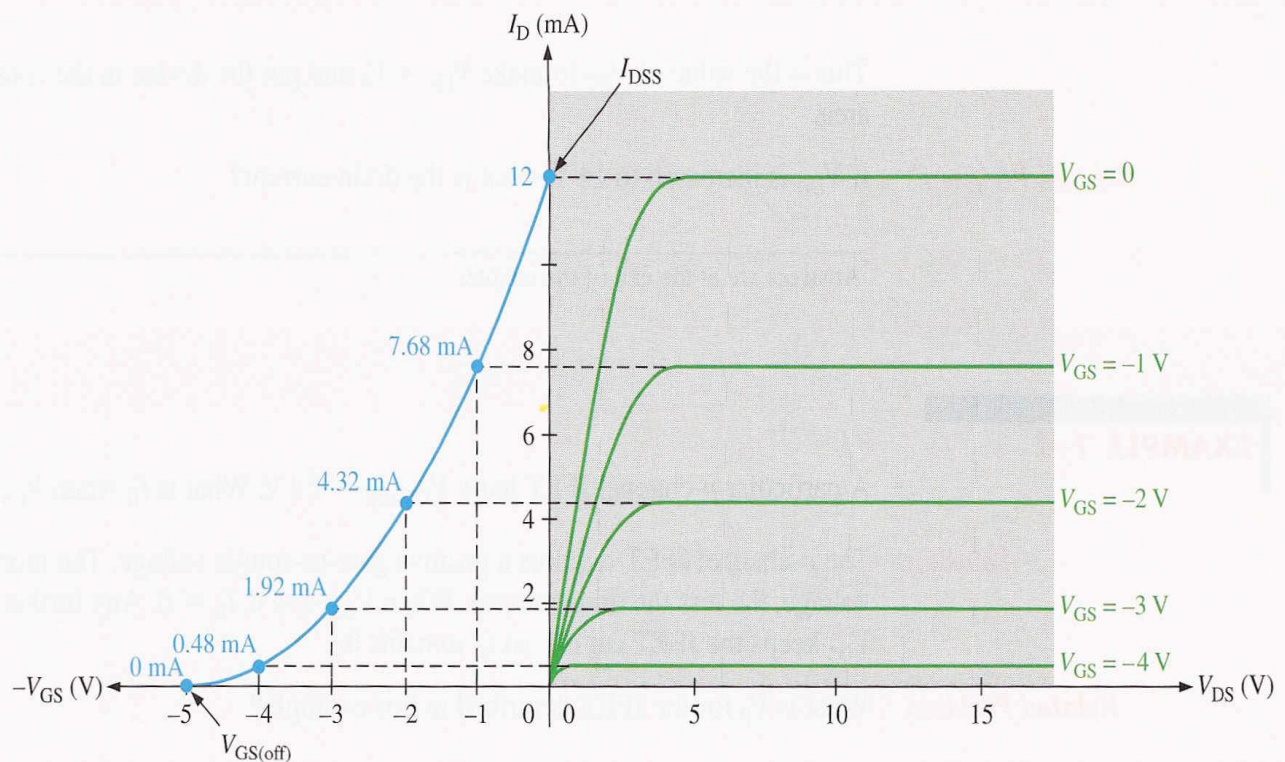
Notice that the bottom end of the curve is at a point on the V_{GS} axis equal to $V_{GS(off)}$, and the top end of the curve is at a point on the I_D axis equal to I_{DSS} . This curve, of course, shows that the operating limits of a JFET are

$$I_D = 0 \quad \text{when } V_{GS} = V_{GS(off)}$$

and

$$I_D = I_{DSS} \quad \text{when } V_{GS} = 0$$

The transfer characteristic curve can be developed from the drain characteristic curves by plotting values of I_D for the values of V_{GS} taken from the family of drain curves at pinch-off, as illustrated in Figure 7–13 for a specific set of curves. Each point on the transfer characteristic curve corresponds to specific values of V_{GS} and I_D on the drain curves. For



▲ **FIGURE 7-13**

Example of the development of an n -channel JFET transfer characteristic curve (blue) from the JFET drain characteristic curves (green).

example, when $V_{GS} = -2$ V, $I_D = 4.32$ mA. Also, for this specific JFET, $V_{GS(off)} = -5$ V and $I_{DSS} = 12$ mA.

A JFET transfer characteristic curve is expressed as

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

With Equation 7-1, I_D can be determined for any V_{GS} if $V_{GS(off)}$ and I_{DSS} are known. These quantities are usually available from the data sheet for a given JFET. Notice the squared term in the equation. Because of its form, a parabolic relationship is known as a *square law*, and therefore, JFETs and MOSFETs are often referred to as *square-law devices*.

The data sheet for a typical JFET series is shown in Figure 7-14.

Example (4 - 3):

The partial data sheet in Figure 7-14 for a 2N5459 JFET indicates that typically $I_{DSS} = 9 \text{ mA}$ and $V_{GS(off)} = -8 \text{ V}$ (maximum). Using these values, determine the drain current for $V_{GS} = 0 \text{ V}$, -1 V , and -4 V .

For $V_{GS} = 0 \text{ V}$,

$$I_D = I_{DSS} = \mathbf{9 \text{ mA}}$$

For $V_{GS} = -1 \text{ V}$, use Equation 7-1.

$$\begin{aligned} I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 = (9 \text{ mA}) \left(1 - \frac{-1 \text{ V}}{-8 \text{ V}} \right)^2 \\ &= (9 \text{ mA})(1 - 0.125)^2 = (9 \text{ mA})(0.766) = \mathbf{6.89 \text{ mA}} \end{aligned}$$

For $V_{GS} = -4 \text{ V}$,

$$I_D = (9 \text{ mA}) \left(1 - \frac{-4 \text{ V}}{-8 \text{ V}} \right)^2 = (9 \text{ mA})(1 - 0.5)^2 = (9 \text{ mA})(0.25) = \mathbf{2.25 \text{ mA}}$$

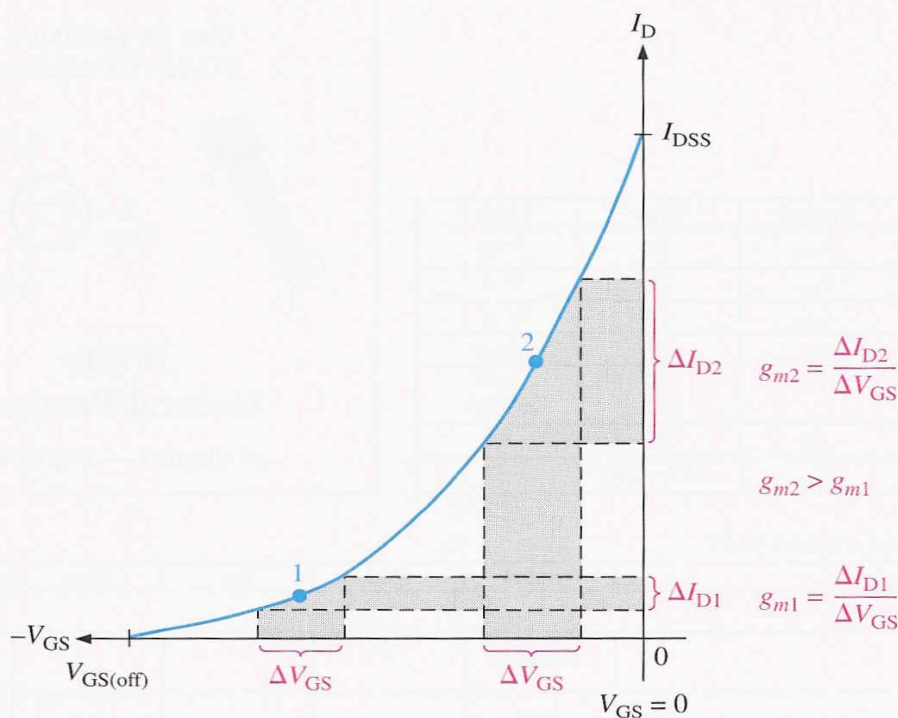
JFET Forward Transconductance

The forward **transconductance** (transfer conductance), g_m , is the change in drain current (ΔI_D) for a given change in gate-to-source voltage (ΔV_{GS}) with the drain-to-source voltage constant. It is expressed as a ratio and has the unit of siemens (S).

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Other common designations for this parameter are g_{fs} and y_{fs} (forward transfer admittance). As you will see in Chapter 8, g_m is important in FET amplifiers as a major factor in determining the voltage gain.

Because the transfer characteristic curve for a JFET is nonlinear, g_m varies in value depending on the location on the curve as set by V_{GS} . The value for g_m is greater near the top of the curve (near $V_{GS} = 0$) than it is near the bottom (near $V_{GS(off)}$), as illustrated in Figure 7–15.



A data sheet normally gives the value of g_m measured at $V_{GS} = 0$ V (g_{m0}). For example, the data sheet for the 2N5457 JFET specifies a minimum g_{m0} (y_{fs}) of 1000 S with $V_{DS} = 15$ V.

Given g_{m0} , you can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following formula:

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)$$

When a value of g_{m0} is not available, you can calculate it using values of I_{DSS} and $V_{GS(off)}$. The vertical lines indicate an absolute value (no sign).

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$

Example (4 - 4) :

The following information is included on the data sheet in Figure 7-14 for a 2N5457 JFET: typically, $I_{DSS} = 3.0 \text{ mA}$, $V_{GS(off)} = -6 \text{ V}$ maximum, and $y_{fs(max)} = 5000 \mu\text{S}$. Using these values, determine the forward transconductance for $V_{GS} = -4 \text{ V}$, and find I_D at this point.

Solution:

$g_{m0} = y_{fs} = 5000 \mu\text{S}$. Use Equation 7-2 to calculate g_m .

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right) = (5000 \mu\text{S}) \left(1 - \frac{-4 \text{ V}}{-6 \text{ V}} \right) = \mathbf{1667 \mu\text{S}}$$

Next, use Equation 7-1 to calculate I_D at $V_{GS} = -4 \text{ V}$.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 = (3.0 \text{ mA}) \left(1 - \frac{-4 \text{ V}}{-6 \text{ V}} \right)^2 = \mathbf{333 \mu\text{A}}$$

JFET BIASING

DC Biasing of a JFET

A JFET may be biased by using either

1. a separate power source V_{GG} as shown in Fig. (a),
2. some form of self-bias as shown in Fig. (b),
3. source bias as in Fig. (c),
4. voltage divider bias as in Fig. (d).

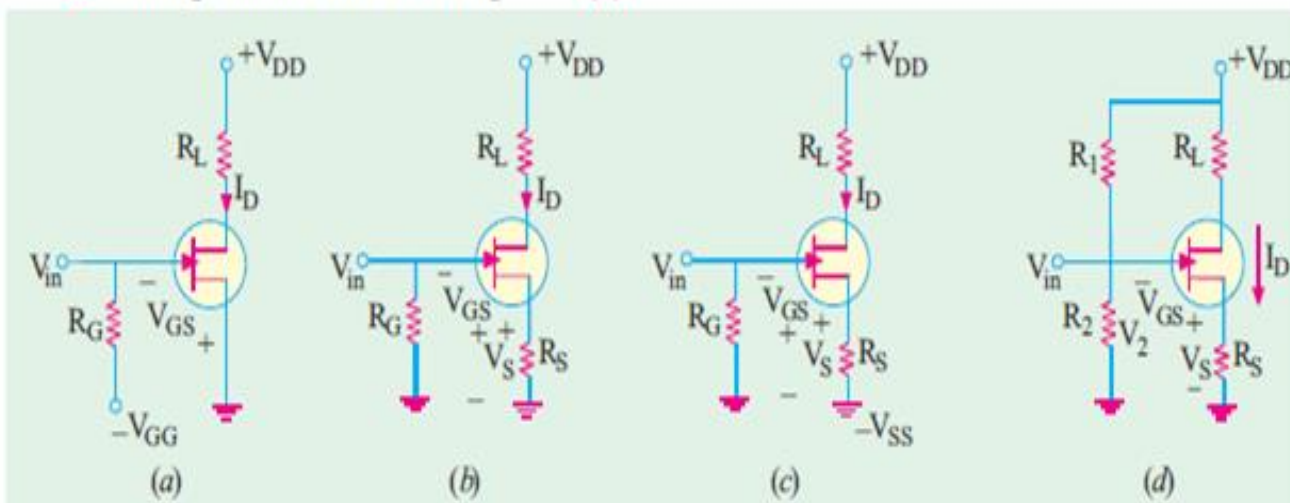


Fig.

The circuit of Fig. (b) is called self-bias circuit because the V_{GS} bias is obtained from the flow of JFET's own drain current I_D through R_S .

$$\therefore V_S = I_D R_S \text{ and } V_{GS} = -I_D R_S$$

The gate is kept at this much negative potential with respect to the ground.

The addition of R_G in Fig. (b), does not upset this dc bias for the simple reason that no gate current flows through it (the gate leakage current is almost zero). Hence, gate is essentially at **dc ground**. Without R_G , gate would be kept 'floating' which could collect charge and ultimately cut-off the JFET.

The resistance R_G additionally serves the purpose of avoiding short-circuiting of the ac input voltage, v_{in} . Moreover, in case leakage current is not totally negligible, R_G would provide it an escape route. Otherwise, the leakage current would build up static charge (voltage) at the gate which could change the bias or even destroy the JFET.

Fig. (c) shows the *source bias* circuit which employs a self-bias resistor R_S to obtain V_{GS} . Here, $V_{SS} = I_D R_S + V_{GS}$ or $V_{GS} = V_{SS} - I_D R_S$.

Fig. (d) shows the familiar voltage divider bias. In this case, $V_2 = V_{GS} + I_D R_S$ or $V_{GS} = V_2 - I_D R_S$

$$\text{Since, } V_2 = V_{DD} \frac{R_2}{R_1 + R_2}$$

$$\therefore V_{GS} = V_{DD} \frac{R_2}{R_1 + R_2} - I_D R_S$$

Self-Bias

Self-bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate-source junction is always reverse-biased. This condition requires a negative V_{GS} for an n -channel JFET and a positive V_{GS} for a p -channel JFET. This can be achieved using the self-bias arrangements shown in Figure 7–16. The gate resistor, R_G , does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V. R_G is necessary only to isolate an ac signal from ground in amplifier applications, as you will see later.

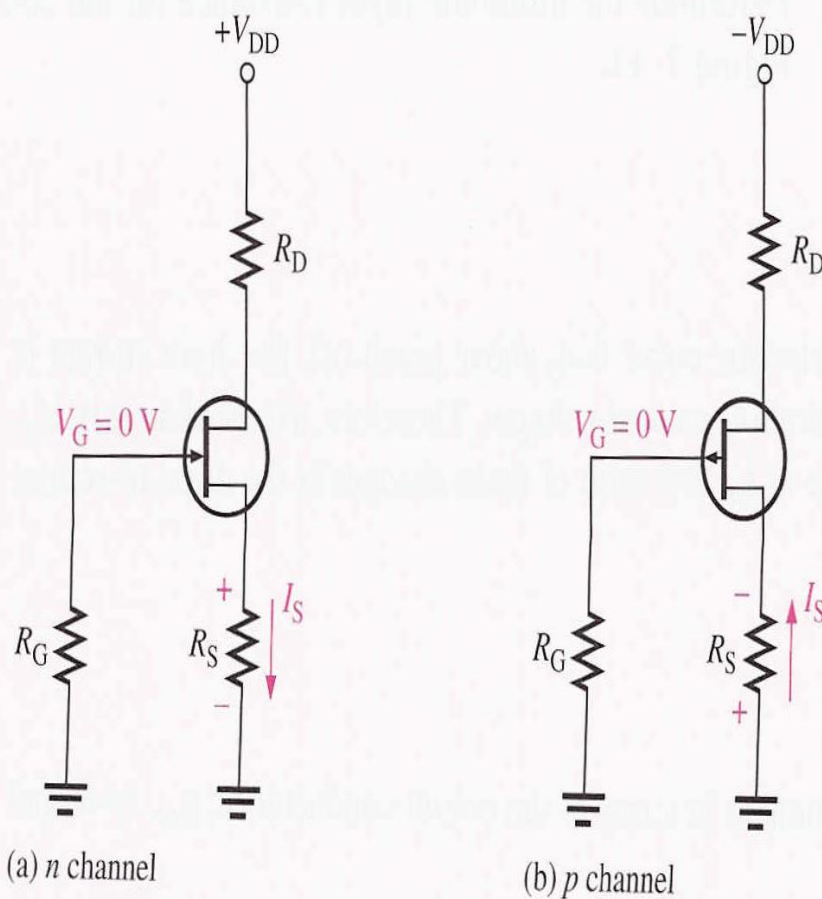


Fig. (4 - 19).self- biased JFET ($I_S = I_D$ in all FETs)

For the n -channel JFET in Figure 7-16(a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = I_D R_S$. The gate-to-source voltage is

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

Thus,

$$V_{GS} = -I_D R_S$$

For the p -channel JFET shown in Figure 7-16(b), the current through R_S produces a negative voltage at the source, making the gate positive with respect to the source. Therefore, since $I_S = I_D$,

$$V_{GS} = +I_D R_S$$

In the following analysis, the n -channel JFET in Figure 7-16(a) is used for illustration. Keep in mind that analysis of the p -channel JFET is the same except for opposite-polarity voltages. The drain voltage with respect to ground is determined as follows:

$$V_D = V_{DD} - I_D R_D$$

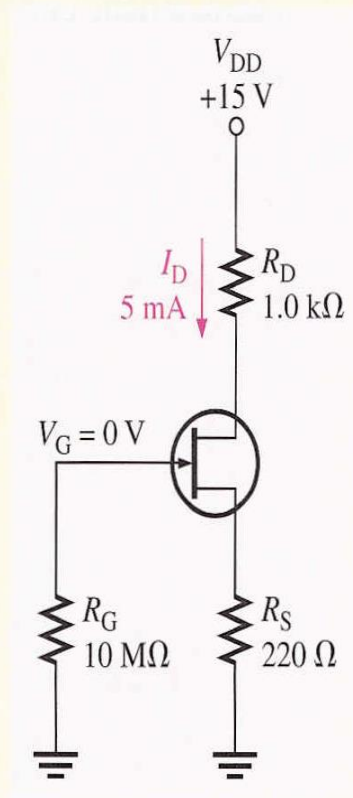
Since $V_S = I_D R_S$, the drain-to-source voltage is

$$V_{DS} = V_D - V_S = V_{DD} - I_D (R_D + R_S)$$

Example (4- 5):

Find V_{DS} and V_{GS} in Figure 7–17. For the particular JFET in this circuit, the internal parameter values such as g_m , $V_{GS(off)}$, and I_{DSS} are such that a drain current (I_D) of approximately 5 mA is produced. Another JFET, even of the same type, may not produce the same results when connected in this circuit due to the variations in parameter values.

► **FIGURE 7–17**



$$V_S = I_D R_S = (5 \text{ mA})(220 \Omega) = 1.1 \text{ V}$$

$$V_D = V_{DD} - I_D R_D = 15 \text{ V} - (5 \text{ mA})(1.0 \text{ k}\Omega) = 15 \text{ V} - 5 \text{ V} = 10 \text{ V}$$

Therefore,

$$V_{DS} = V_D - V_S = 10 \text{ V} - 1.1 \text{ V} = \mathbf{8.9 \text{ V}}$$

Since $V_G = 0 \text{ V}$,

$$V_{GS} = V_G - V_S = 0 \text{ V} - 1.1 \text{ V} = \mathbf{-1.1 \text{ V}}$$

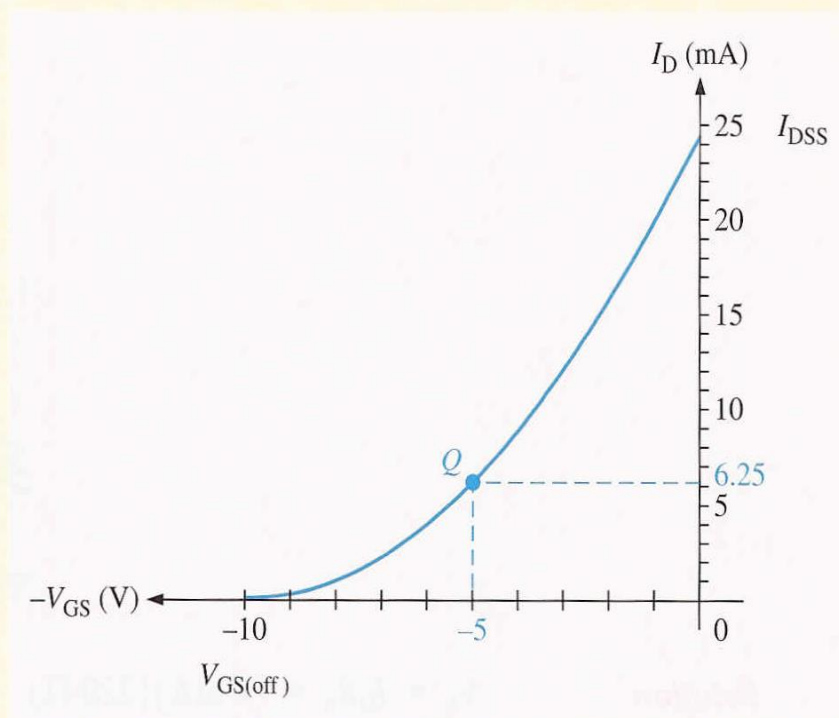
Setting the Q-Point of a Self-Biased JFET

The basic approach to establishing a JFET bias point is to determine I_D for a desired value of V_{GS} or vice versa. Then calculate the required value of R_S using the following relationship. The vertical lines indicate an absolute value.

$$R_S = \left| \frac{V_{GS}}{I_D} \right|$$

For a desired value of V_{GS} , I_D can be determined in either of two ways: from the transfer characteristic curve for the particular JFET or, more practically, from Equation 7-1 using I_{DSS} and $V_{GS(off)}$ from the JFET data sheet. The next two examples illustrate these procedures.

Determine the value of R_S required to self-bias an n -channel JFET that has the transfer characteristic curve shown in Figure 7-18 at $V_{GS} = -5$ V.



From the graph, $I_D = 6.25$ mA when $V_{GS} = -5$ V. Calculate R_S .

$$R_S = \left| \frac{V_{GS}}{I_D} \right| = \frac{5 \text{ V}}{6.25 \text{ mA}} = 800 \, \Omega$$

Example (4-6):

Determine the value of R_S required to self-bias a p -channel JFET with $I_{DSS} = 25 \text{ mA}$ and $V_{GS(off)} = 15 \text{ V}$. V_{GS} is to be 5 V .

Use Equation 7-1 to calculate I_D .

$$\begin{aligned} I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 = (25 \text{ mA}) \left(1 - \frac{5 \text{ V}}{15 \text{ V}} \right)^2 \\ &= (25 \text{ mA})(1 - 0.333)^2 = 11.1 \text{ mA} \end{aligned}$$

Now, determine R_S .

$$R_S = \left| \frac{V_{GS}}{I_D} \right| = \frac{5 \text{ V}}{11.1 \text{ mA}} = \mathbf{450 \, \Omega}$$

Graphical Analysis of a Self-Biased JFET

You can use the transfer characteristic curve of a JFET and certain parameters to determine the Q-point (I_D and V_{GS}) of a self-biased circuit. A circuit is shown in Figure 7-20(a), and a transfer characteristic curve is shown in Figure 7-20(b). If a curve is not available from a data sheet, you can plot it from Equation 7-1 using data sheet values for I_{DSS} and $V_{GS(off)}$.

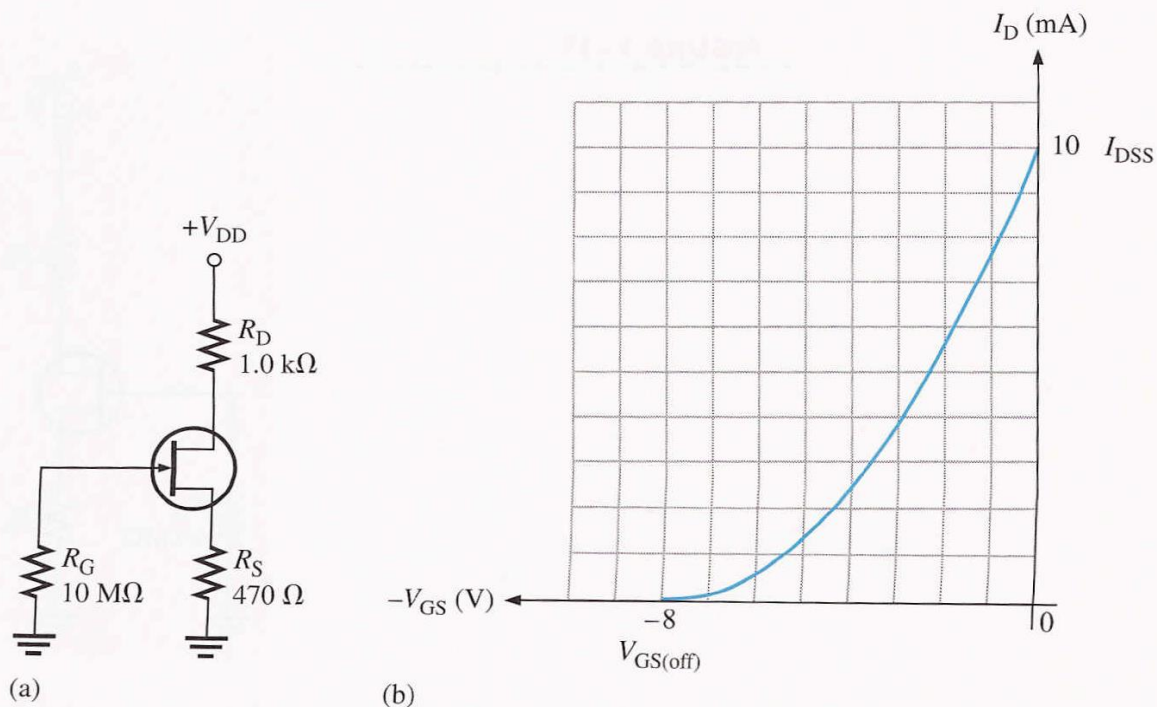


Fig. (4 - 22).Self- biased JFET and its transfer characteristic curve

To determine the Q-point of the circuit in Figure 7-20(a), a self-bias dc load line is established on the graph in part (b) as follows. First, calculate V_{GS} when I_D is zero.

$$V_{GS} = -I_D R_S = (0) (470 \, \Omega) = 0 \, \text{V}$$

This establishes a point at the origin on the graph ($I_D = 0$, $V_{GS} = 0$). Next, calculate V_{GS} when $I_D = I_{DSS}$. From the curve in Figure 7-20(b), $I_{DSS} = 10 \, \text{mA}$.

$$V_{GS} = -I_D R_S = -(10 \, \text{mA}) (470 \, \Omega) = -4.7 \, \text{V}$$

This establishes a second point on the graph ($I_D = 10 \, \text{mA}$, $V_{GS} = -4.7 \, \text{V}$). Now, with two points, the load line can be drawn on the transfer characteristic curve as shown in Figure 7-21. The point where the line intersects the transfer characteristic curve is the Q-point of the circuit as shown.

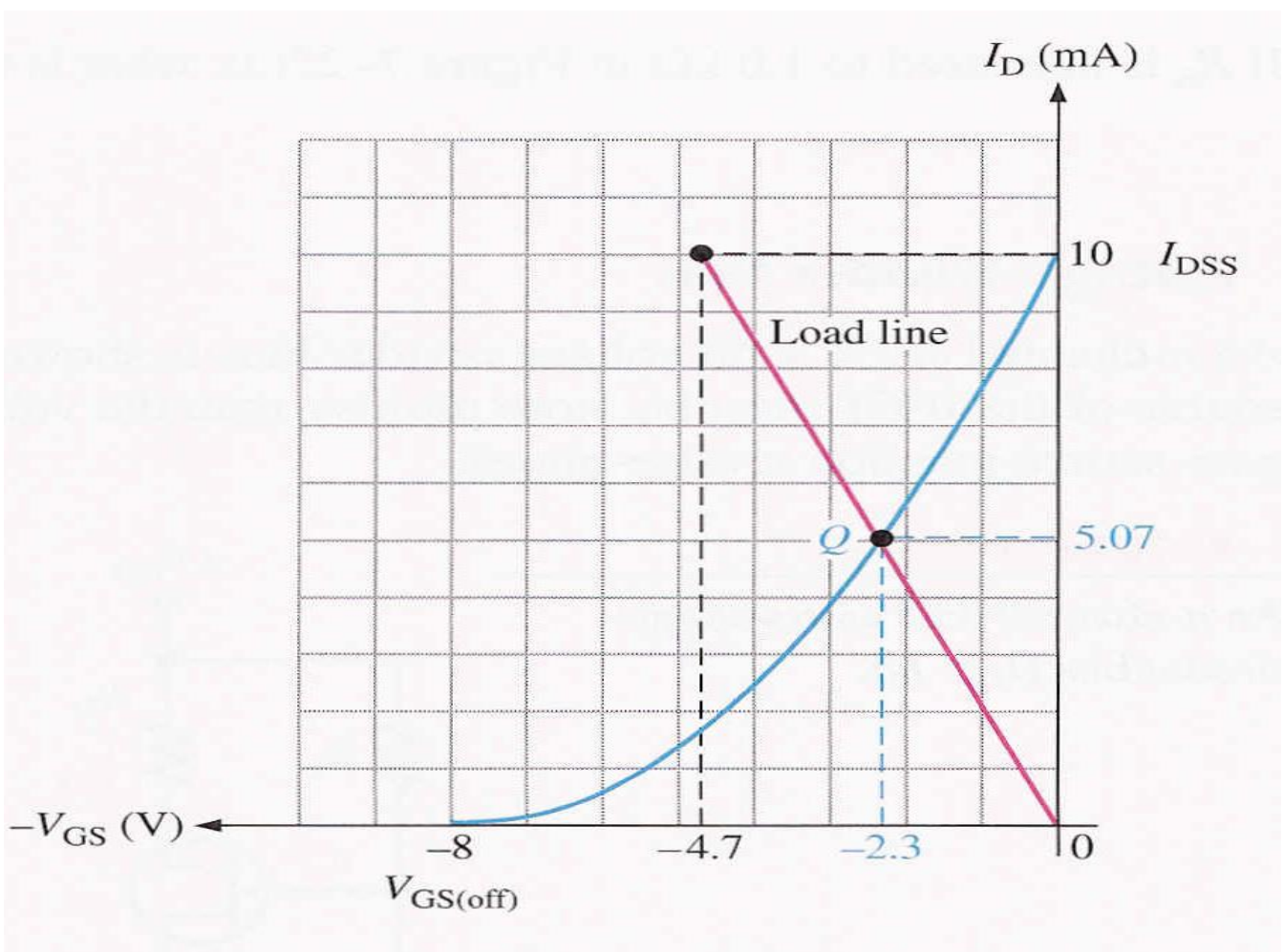


Fig. (4 - 23).The intersection of the self- bias DC load line and the transfer characteristic curve is the Q-point.

Example (4- 7):

Determine the Q-point for the JFET circuit in Figure 7–22(a). The transfer characteristic curve is given in Figure 7–22(b).

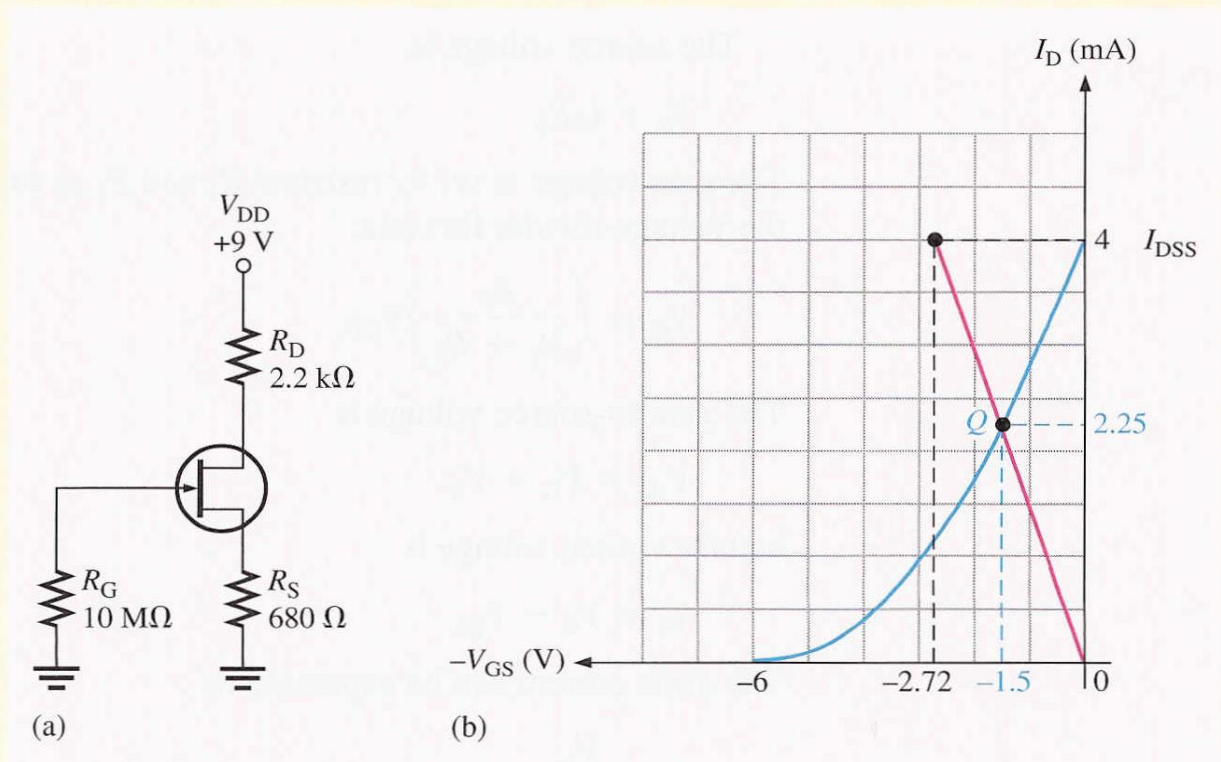


Fig. (4 - 24)

Solution:

For $I_D = 0$,

$$V_{GS} = -I_D R_S = (0)(680\text{ }\Omega) = 0\text{ V}$$

This gives a point at the origin. From the curve, $I_{DSS} = 4\text{ mA}$; so $I_D = I_{DSS} = 4\text{ mA}$.

$$V_{GS} = -I_D R_S = -(4\text{ mA})(680\text{ }\Omega) = -2.72\text{ V}$$

This gives a second point at 4 mA and -2.72 V . A line is now drawn between the two points, and the values of I_D and V_{GS} at the intersection of the line and the curve are taken from the graph, as illustrated in Figure 7–22(b). The Q-point values from the graph are

$$I_D = 2.25\text{ mA}$$

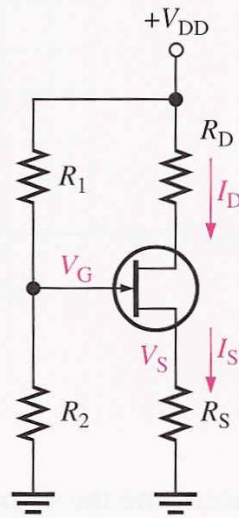
$$V_{GS} = -1.5\text{ V}$$

Voltage-Divider Bias

An n -channel JFET with voltage-divider bias is shown in Figure 7–23. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased.

► **FIGURE 7–23**

An n -channel JFET with voltage-divider bias ($I_S = I_D$).



The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage-divider formula:

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$

The gate-to-source voltage is

$$V_{GS} = V_G - V_S$$

and the source voltage is

$$V_S = V_G - V_{GS}$$

The drain current can be expressed as

$$I_D = \frac{V_S}{R_S}$$

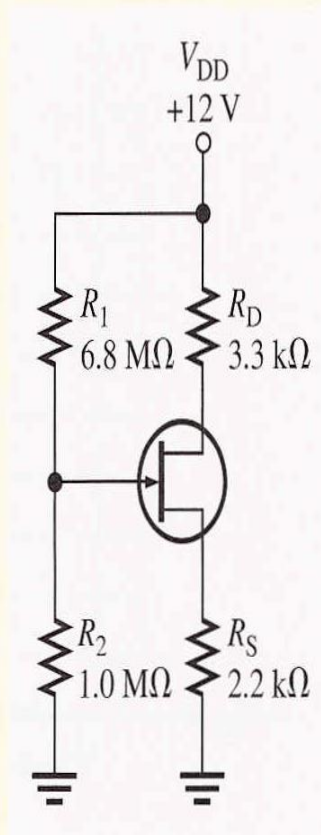
Substituting for V_S ,

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

Example (4 - 8) :

Determine I_D and V_{GS} for the JFET with voltage-divider bias in Figure 7-24, given that for this particular JFET the internal parameter values are such that $V_D \cong 7 \text{ V}$.

► **FIGURE 7-24**



$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12 \text{ V} - 7 \text{ V}}{3.3 \text{ k}\Omega} = \frac{5 \text{ V}}{3.3 \text{ k}\Omega} = \mathbf{1.52 \text{ mA}}$$

Calculate the gate-to-source voltage as follows:

$$V_S = I_D R_S = (1.52 \text{ mA})(2.2 \text{ k}\Omega) = 3.34 \text{ V}$$

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{1.0 \text{ M}\Omega}{7.8 \text{ M}\Omega} \right) 12 \text{ V} = 1.54 \text{ V}$$

$$V_{GS} = V_G - V_S = 1.54 \text{ V} - 3.34 \text{ V} = \mathbf{-1.8 \text{ V}}$$

If V_D had not been given in this example, the Q-point values could not have been found without the transfer characteristic curve.

Graphical Analysis of a JFET with Voltage-Divider Bias

An approach similar to the one used for self-bias can be used with voltage-divider bias to graphically determine the Q-point of a circuit on the transfer characteristic curve.

In a JFET with voltage-divider bias when $I_D = 0$, V_{GS} is not zero, as in the self-biased case, because the voltage divider produces a voltage at the gate independent of the drain current. The voltage-divider dc load line is determined as follows.

For $I_D = 0$,

$$V_S = I_D R_S = (0)R_S = 0 \text{ V}$$

$$V_{GS} = V_G - V_S = V_G - 0 \text{ V} = V_G$$

Therefore, one point on the line is at $I_D = 0$ and $V_{GS} = V_G$.

For $V_{GS} = 0$,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S}$$

A second point on the line is at $I_D = V_G/R_S$ and $V_{GS} = 0$. The generalized dc load line is shown in Figure 7–25. The point at which the load line intersects the transfer characteristic curve is the Q-point.

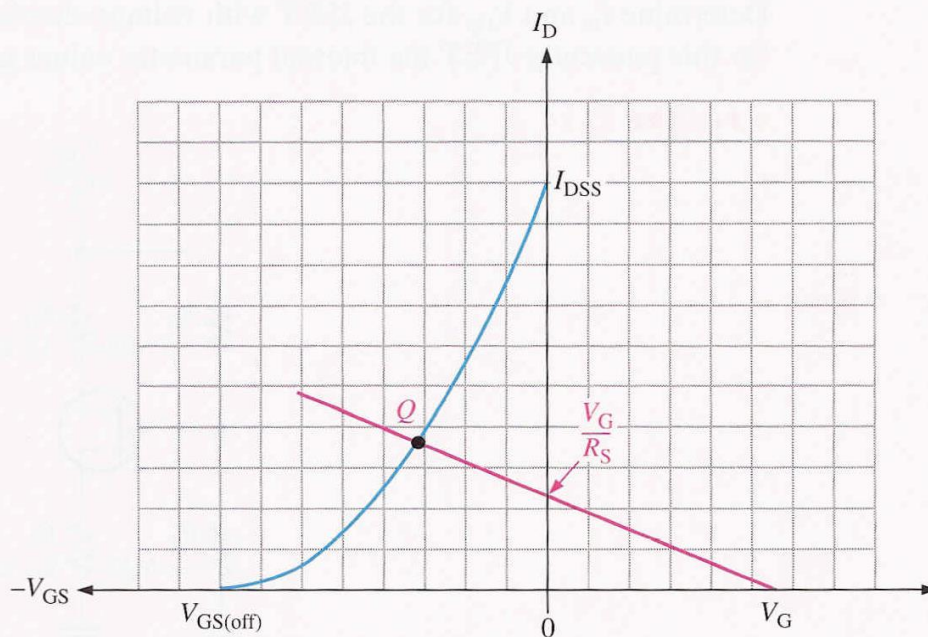


Fig.(4- 27). Generalized DC load line for JFET with voltage- divider bias.

Example (4- 9):

Determine the approximate Q-point for the JFET with voltage-divider bias in Figure 7-26(a), given that this particular device has a transfer characteristic curve as shown in Figure 7-26(b).

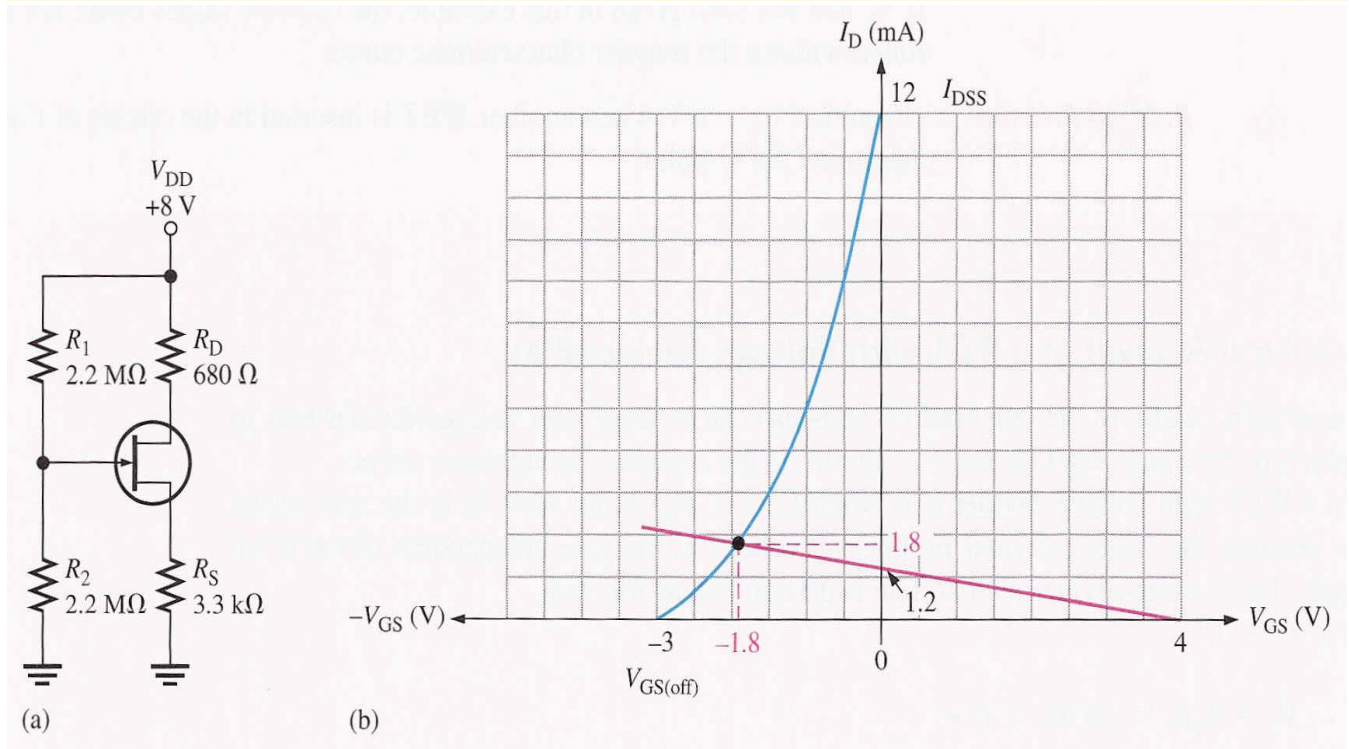


Fig. (4- 30).

First, establish the two points for the bias line. For $I_D = 0$,

$$V_{GS} = V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{2.2 \text{ M}\Omega}{4.4 \text{ M}\Omega} \right) 8 \text{ V} = 4 \text{ V}$$

The first point is at $I_D = 0$ and $V_{GS} = 4 \text{ V}$. For $V_{GS} = 0$,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S} = \frac{4 \text{ V}}{3.3 \text{ k}\Omega} = 1.2 \text{ mA}$$

The second point is at $I_D = 1.2 \text{ mA}$ and $V_{GS} = 0$.

The load line is drawn in Figure 7-26(b), and the approximate Q-point values of $I_D \cong 1.8 \text{ mA}$ and $V_{GS} \cong -1.8 \text{ V}$ are picked off the graph, as indicated.

THE MOSFET

The MOSFET (metal oxide semiconductor field-effect transistor) is another category of field-effect transistor. The MOSFET differs from the JFET in that it has no *pn* junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. The two basic types of MOSFETs are

depletion (D) and enhancement (E). Because of the insulated gate, these devices are sometimes called IGFETs.

4-2: Applications: Power Amplifier:

The main characteristics of the power amplifiers are :

1. Linearity : it preserve the details of signal waveform , $V_o(t) = A V_i(t)$
2. Efficiency (η) : it is the conversion of DC power of supply into signal power delivered to load

$$\eta = \frac{\text{Signal power delivered to load}}{\text{DC power supplied to o/p circuit}}$$

3. Output power.
4. Signal gain.

In general, there is a tradeoff between these characteristics. For example, improving amplifier's linearity will degrade its efficiency. Therefore knowing the importance degree of each one of these characteristics is an essential step in designing an Amplifier. This can be juggled based on the application. As an example high output power Amplifier is used in the transmitter side of a transceiver, whereas high linear amplifier used in the receiver side.

Power Amplifiers classes :

It classified according to :

1. Circuit configuration.
2. Method of operation.

Power amplifier class	notes	
A	Linear	High linearity, less efficiency
B		less linearity, high efficiency
AB		Compromise between A &B
C	Non linear	Output current is zero for more than $\frac{1}{2}$ of input signal
D		
E		
F		Highest efficiency η