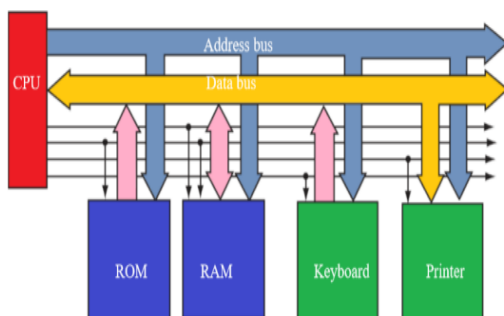
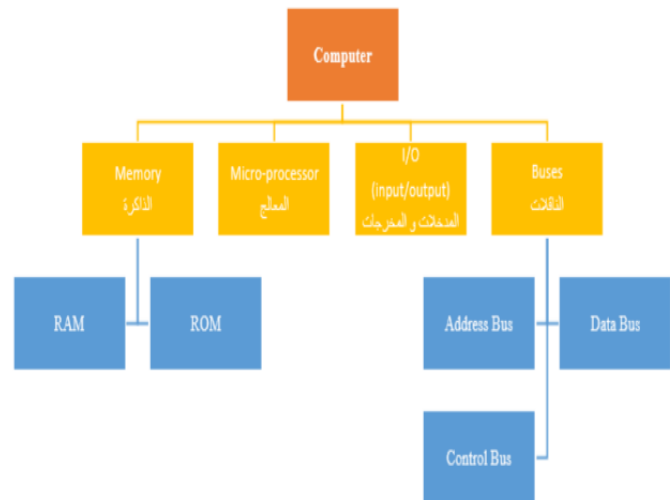


- Brief History of the CPU ▪ 4004 ▪ 8008 ▪ 8080 ▪ 8085 ▪ 8086 ▪ 8088 ▪ 80286 ▪ 80386 ▪ 80486 ▪ Pentium ▪ Pentium Pro
- Pentium II ▪ Pentium III ▪ Pentium 4 ▪ Itanium

Some Important Terminology

memory	Size
Bit	1 bit
Nibble	4 bit
Byte	8 bit (1 byte)
Word	16-bit (2 bytes)
kilobyte (KB)	2 ¹⁰ bytes (1024 byte)
megabyte (MB)	2 ²⁰ bytes (1024 KB)
gigabyte (GB)	2 ³⁰ bytes (1024 MB)
terabyte (TB)	2 ⁴⁰ bytes (1024 GB)

Internal Organization of Computers



memory الذاكرة



RAM (ذاكرة مؤقتة)	ROM (ذاكرة دائمة)
- RAM stands to Random Access Memory (called Read / Write Memory) - RAM is used by the computer for temporary storage of programs that it is running - RAM is sometimes called Volatile memory	- ROM stands for read-only memory - It contains programs and information essential to operation of the computer - It is called nonvolatile memory

1. The 4004 Microprocessor ▪ The world's first microprocessor the Intel 4004. ▪ A 4-bit microprocessor-programmable controller on a Chip ▪ Addressed 4096, 4-bit-wide memory locations. ▪ The 4004-instruction set contained 45 instructions. ▪ Main problems with early microprocessor were : • speed(slow) • word width(4bits) • and memory size(4KB).

Intel 4004

Introduced in 1971

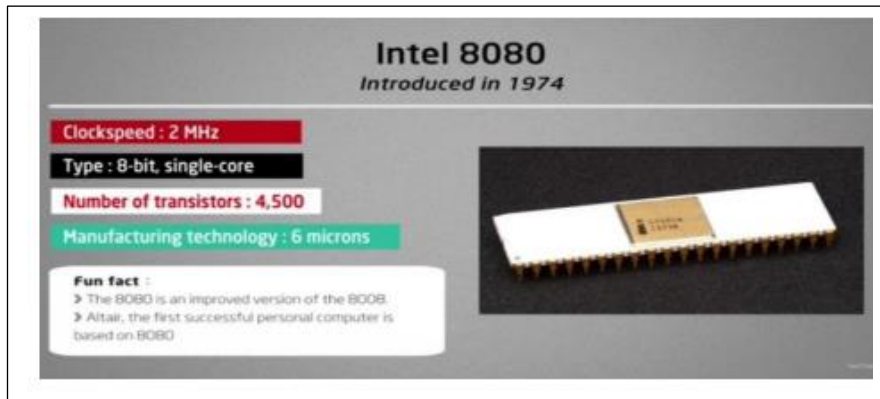
- Clockspeed :** 108 -740 KHz
- Type :** 4-bit, single-core
- Number of transistors :** 2,300
- Manufacturing technology :** 10 microns

Fun fact :

- The 4004 is Intel's first microprocessor.
- It powered the Busicom calculator and paved the way for the personal computer

2. The 8008 Microprocessor ▪ Intel released 8008 in 1971. ▪ extended 8-bit version of 4004 microprocessor. ▪ Addressed expanded memory of 16K bytes.

3. The 8080 Microprocessor ▪ Intel introduced 8080 microprocessors in 1973. ▪ first of the 8-bit general purpose microprocessor ▪ 8080 addressed four times more memory. 64K bytes.

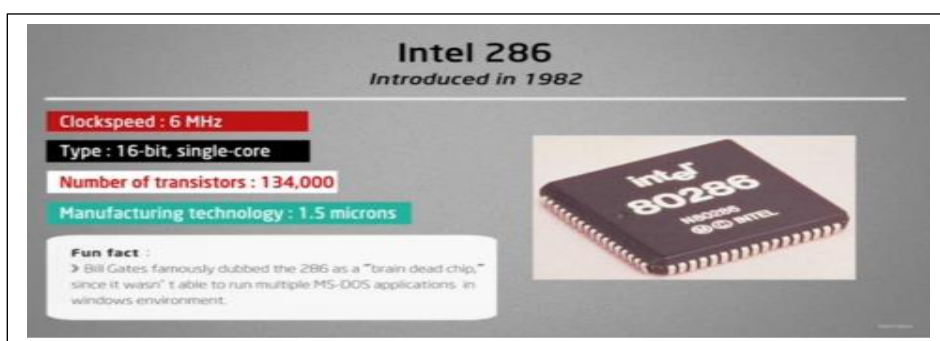


4. The 8085 Microprocessor ▪ In 1977 Intel Corporation introduced 8085 (an updated version of the 8080) ▪ Last 8-bit, general-purpose microprocessor developed by Intel. ▪ Main advantages of 8085 were its: • internal clock generator • higher clock frequency

5. The 8086 and 8088 Microprocessor ▪ In 1978 Intel released the 8086; a year or so later, it released the 8088. ▪ Both devices are 16-bit microprocessors. ▪ 8086 & 8088 addressed 1M byte of memory. ▪ The number of instructions increased. ▪ Another feature was a 4- or 6-byte instruction cache or queue that prefetched instructions before they were executed



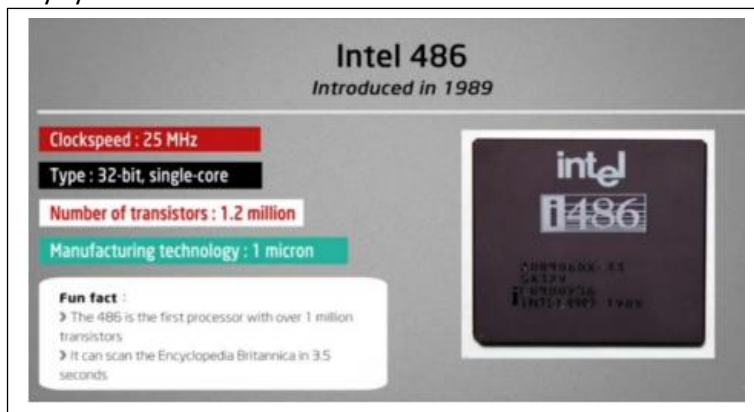
6. The 80286 Microprocessor ▪ Intel introduced the 80286 in 1983 (an updated 8086) ▪ Almost identical to the 8086 and 8088. ▪ Addressed 16M-byte memory system instead of a 1M-byte system



7. The 80386 Microprocessor ▪ Applications demanded faster microprocessor speeds, more memory, and wider data paths. Led to the 80386 in 1986 by Intel. ▪ major overhaul of 16-bit 8086–80286 architecture ▪ Intel's first practical microprocessor to contain a 32-bit data bus and 32-bit memory address



8. The 80486 Microprocessor ▪ In 1989 Intel released the 80486. ▪ 80386-like microprocessor. ▪ 8K-byte cache memory system.



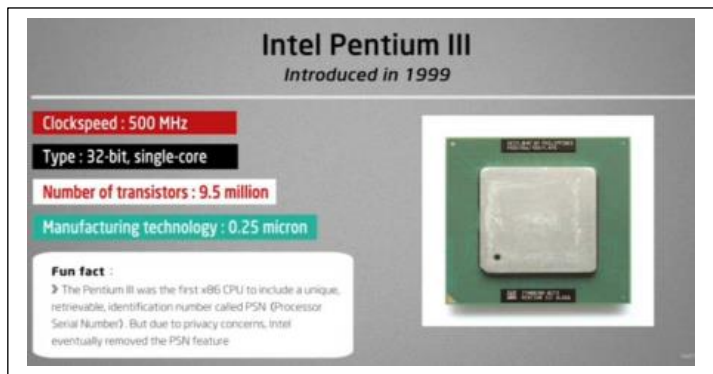
9. The Pentium Microprocessor ▪ Originally labeled the P5 or 80586. ▪ Cache size was increased to 16K bytes from the 8K cache found in 80486. • 8K-byte instruction cache • 8K-byte data cache. ▪ Memory system up to 4G bytes. ▪ Data bus width increased to a full 64 bits.

10. The Pentium Pro Microprocessor ▪ A recent entry, formerly named the P6. ▪ Pentium Pro contains 2 levels of cache. • Internal 16K level-one (L1) cache. 8K data, 8K for instructions • 256K level-two (L2) cache • Pentium Pro uses three execution engines, to execute up to three instructions at a time • Pentium Pro can address 4G-byte or a 64G-byte memory system.

11. The Pentium II Microprocessor ▪ Pentium II, released 1997. ▪ L2 cache on main circuit board of not fast enough to function properly with Pentium II ▪ The Pentium II incorporated Intel technology.



12. The Pentium III Microprocessor ▪ Faster core than Pentium II ▪ Additional FP instructions to support 3D graphics



13. The Pentium 4 Microprocessor ▪ most recent version of Pentium called Core2. ▪ uses Intel P6 architecture. ▪ Pentium 4 available to 3.2 GHz and faster

14. The Future Microprocessor (Itanium) ▪ This new generation of Intel processor makes use of a 64-bit organization with the IA-64 architecture. ▪ The Itanium architecture allows greater parallelism than traditional architectures. ▪ 128 general-purpose integer and 128 floating-point registers; 64 predicate registers. ▪ Many execution units to ensure enough hardware resources for software.

1. AX Register: For 16-bit operations, AX is called the accumulator register that stores operands for arithmetic operations.

2. BX Register: This register is mainly used as a base register. It holds the starting base location of a memory region within a data segment.

3. CX Register: It is defined as a counter. It is primarily used in loop instruction to store loop counter.

4. DX Register: DX register is used to contain I/O port address for I/O instruction and DL. These register pairs are referred to the AX, BX, CX, and DX resp

❖ Stack Pointer Register The stack pointer (SP) register contains the 16-bit offset from the start of the segment to the memory location where a word was most recently stored on the stack.

❖ Flag Register A 16-bit flag register is a flip-flop which indicates some condition produced by the execution of an instruction or controls certain operations of the EU. They are modified automatically by CPU after mathematical operations. It has 9 flags and they are divided into two categories:

1. Conditional Flags

Conditional flags represent result of last arithmetic or logical instructions.

- Carry Flag (CF): This flag will be set to one if the arithmetic operation produces the carry in MSB position. It is also used in multiple-precision arithmetic.

- Auxiliary Flag (AF): If an operation performed in ALU generates a carry/borrow from lower nibble (i.e. D0 – D3) to upper nibble (i.e. D4 – D7), the AF flag is set i.e. carry given by D3 bit to D4 is AF flag. This is not a general-purpose flag; it is used internally by the processor to perform Binary to BCD conversion.

- Parity Flag (PF): This flag is used to indicate the parity of result. If lower order 8- bits of the result contains even number of 1's, the Parity Flag is set to one and for odd number of 1's, the Parity Flag is reset i.e. zero.

- Zero Flag (ZF): It is set to one; if the result of arithmetic or logical operation is zero else it is reset.

- Sign Flag (SF): In sign magnitude format the sign of number is indicated by MSB bit. If the result of operation is negative, sign flag is set to one.

Overflow Flag (OF): It occurs when signed numbers are added or subtracted. An OF indicates that the result has exceeded the capacity of machine.

2. Control Flags

Control flags are intentionally set or reset to control certain operations of the processor with specific instructions put in the program from the user. Control flags are as follows:

- Trap Flag (TF): It is used for single step control. It allows user to execute one instruction of a program at a time for debugging. When trap flag is set, program can be run in single step mode.
- Interrupt Flag (IF): It is an interrupt enable/disable flag, i.e. used to allow/prohibit the interruption of a program. If it is set, the maskable interrupt is enabled and if it is reset, the interrupt is disabled.

3. Direction Flag (DF): It is used in string operation. If it is set, string bytes are accessed from higher memory address to lower memory address. When it is reset, the string bytes are accessed from lower memory address to higher memory address.

Example 1

MOV CL, 03 H

Moves the 8-bit data 03 H into CL

Example 2

MOV DX, 0525 H

Moves the 16-bit data 0525 H into DX

In the above two examples, the source operand is in immediate mode and the destination operand is in register mode

Example 1

MOV DX (Destination Register), CX (Source Register)

Which moves 16-bit content of CX into DX

. Example 2

MOV CL, DL

Moves 8-bit contents of DL into CL

MOV BX, CH is an illegal instruction.

* The register sizes must be the same.

Example: MOV AX, [6107 h]

SUB [6107 h], CL

Here, data resides in a memory location in the data segment, whose

The default segment is always DS.

physical address may be computed using 6107 h as the offset address and content of DS as segment address. The physical address , here , is : $\text{physical address} = \text{DS} * 10 \text{ h} + 6107 \text{ h}$

. But by using a segment override prefix (SOP) in the instruction, any of the four segment registers can be referenced

Example

MOV [DI], BX

Indirect

If [DS] = 5004, [DI] = 0020, [Bx] = 2456 ,PA(Physical address)=50060.

The content of BX (2456) is moved to memory locations 50060 H and 50061 H.

Here memory is [BX] or [BP].

Example:

MOV AX , [BX] ; segment is DS

SBB [BP] ,CX ; segment is SS

INC wordptr[BX] ; segment is SS

