



كلية المأمون الجامعة
قسم هندسة تقنيات الحاسوب
المرحلة الاولى / الالكترونيك الرقمي

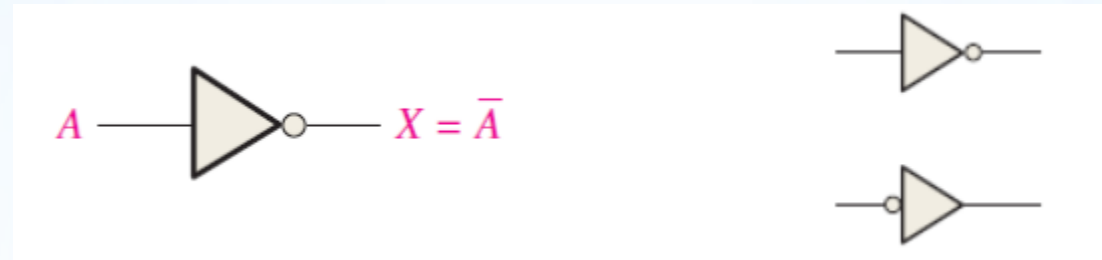
*Lecture 3

Logic Gates

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*The Inverter (NOT) Gate

- * The inverter (NOT circuit) performs the operation called inversion or complementation. The inverter changes one logic level to the opposite level. In terms of bits, it changes a 1 to a 0 and a 0 to a 1.

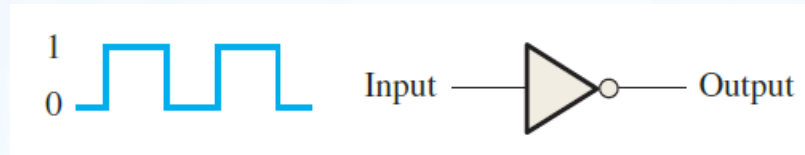


- * This operation is summarized in Table below, a table such as this is called a truth table.

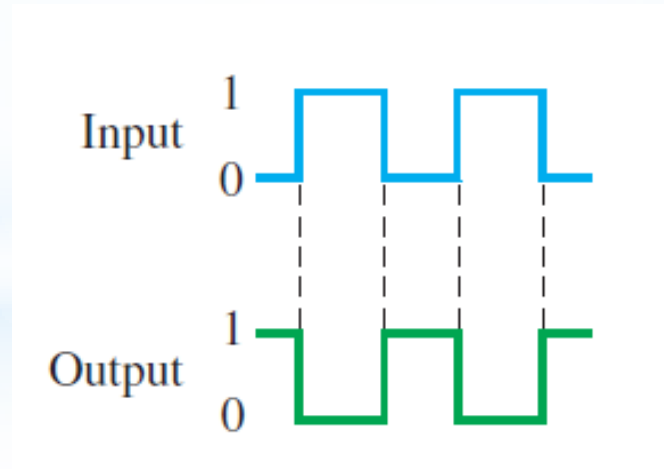
Inverter truth table.

Input	Output
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)

EXAMPLE: A waveform is applied to an inverter in Figure below. Determine the output waveform corresponding to the input and show the timing diagram. According to the placement of the bubble, what is the active output state?



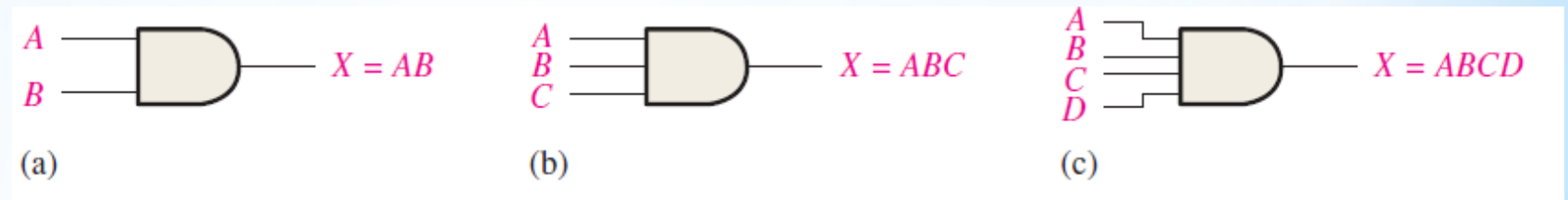
***Solution:** The output waveform is exactly opposite to the input (inverted), as shown in Figure below, which is the basic timing diagram. The active or asserted output state is 0.



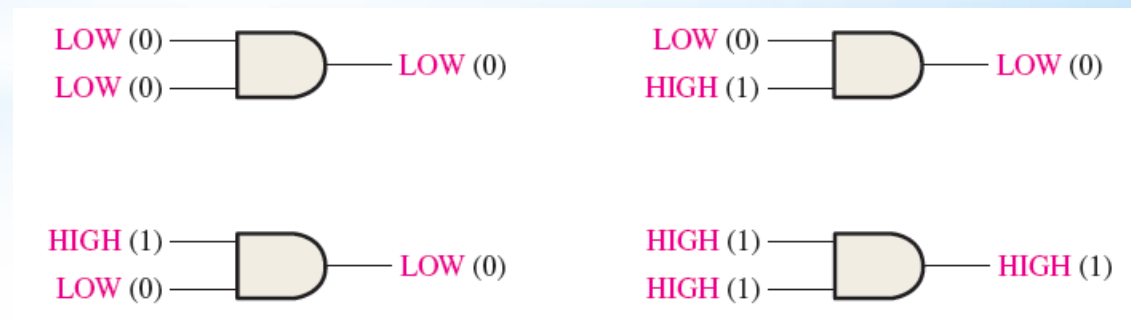
*The AND Gate

The AND gate can have two or more inputs and performs what is known as logical multiplication.

Figure below shows the AND gate logic symbol with **two**, **three**, and **four** input variables and the output variables indicated.



* Figure below illustrates a 2-input AND gate with all four possibilities of input combinations and the resulting output for each.

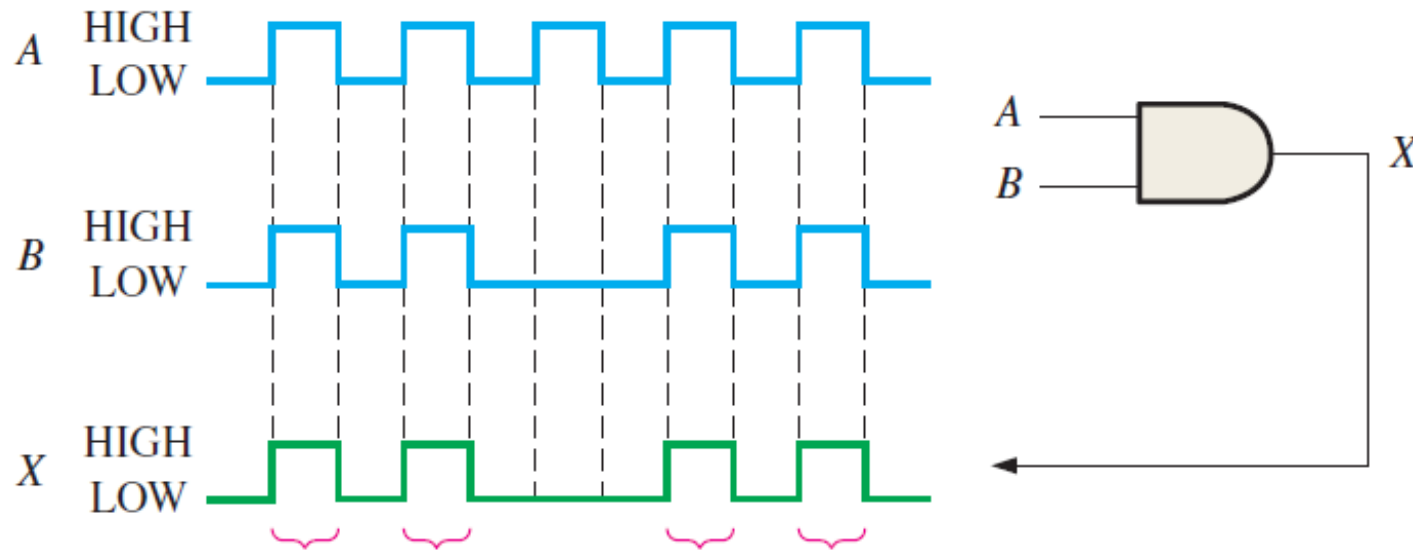


* Truth table for a 2-input AND gate

* For two input variables: $N = 2^2 = 4$ combinations

* For three input variables: $N = 2^3 = 8$ combinations

* For four input variables: $N = 2^4 = 16$ combinations



A and B are both HIGH during these four time intervals;
therefore, X is HIGH.

Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

1 = HIGH, 0 = LOW

* The OR Gate

The OR gate can have two or more inputs and performs what is known as logical addition.

Figure below shows the OR gate logic symbol with **two**, **three**, and **four** input variables and the output variables labeled.

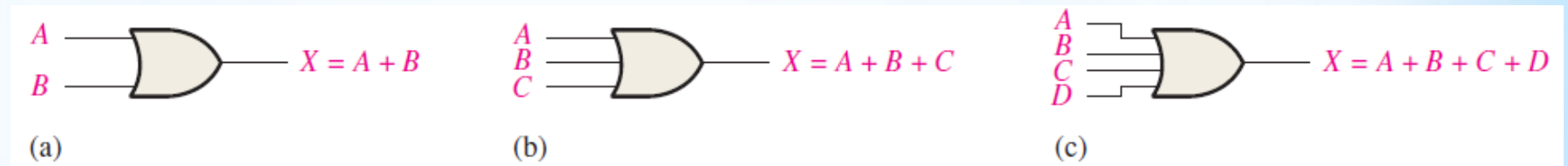
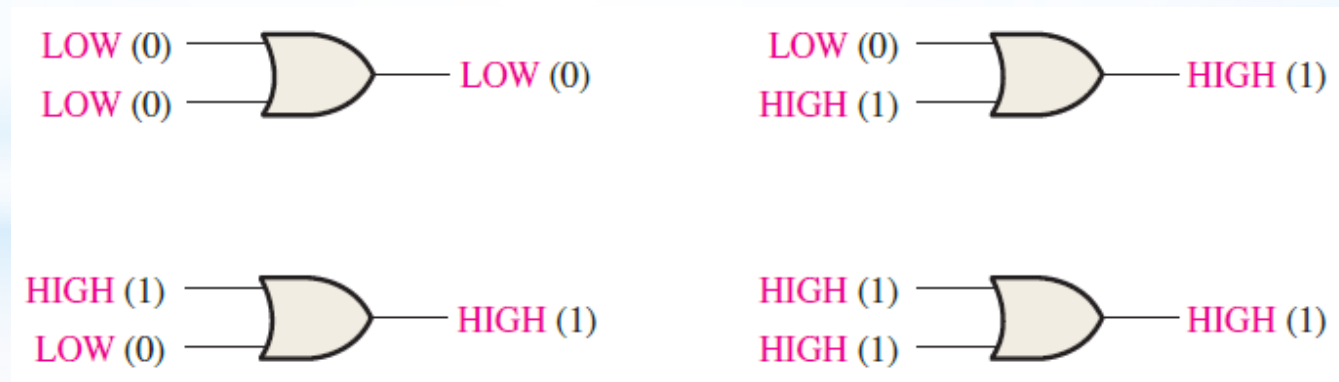
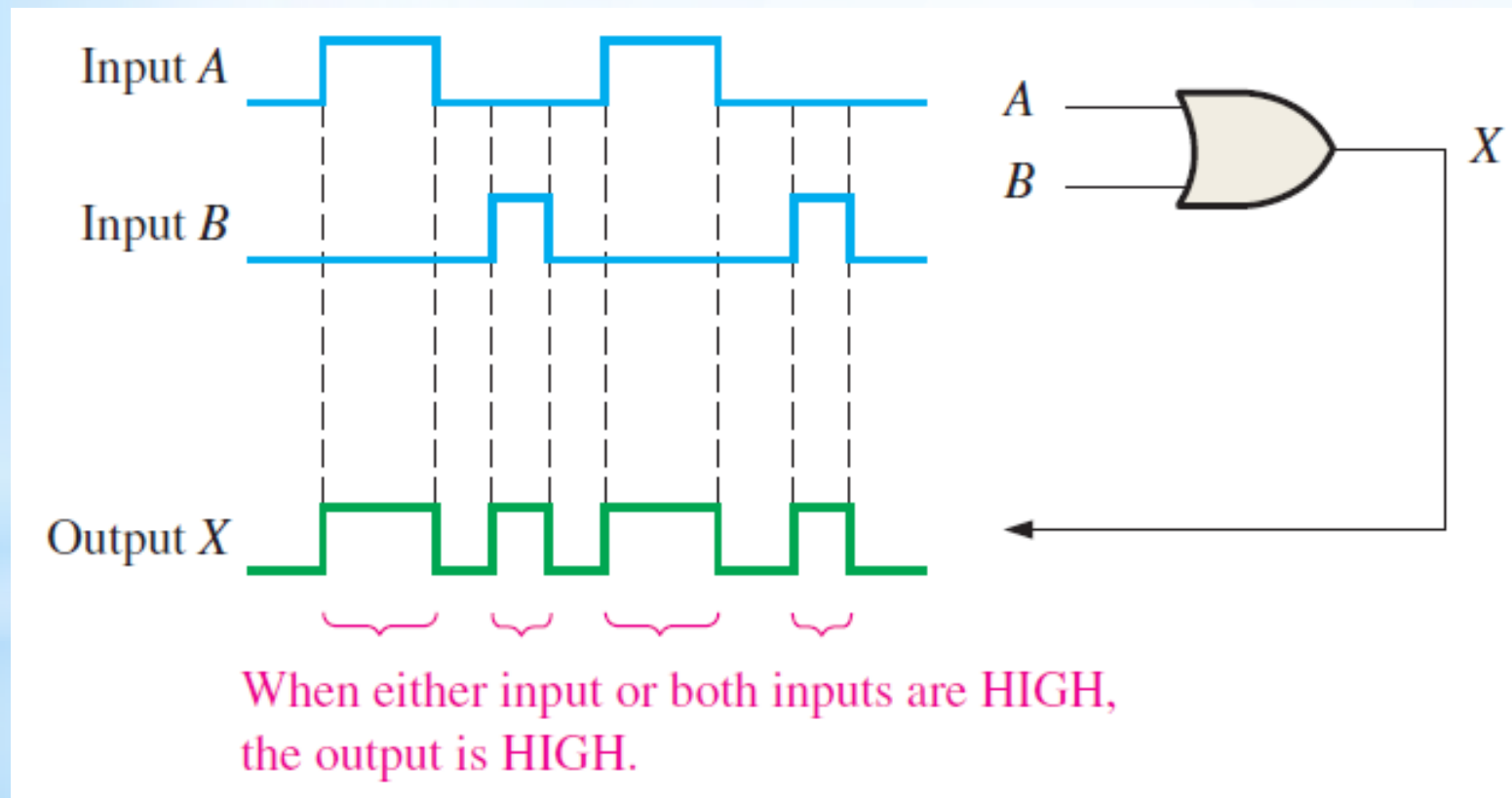


Figure below illustrates a **2-input OR** gate for all four possibilities of input combinations.



***The operation of a 2-input OR gate is described in Table below.**

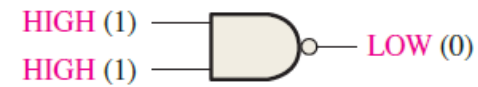
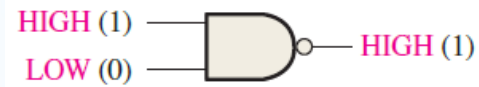
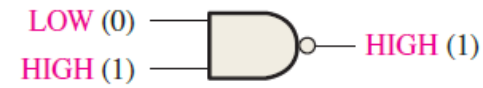
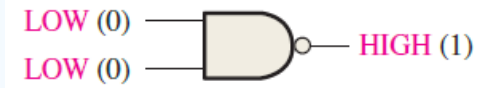


Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

1 = HIGH, 0 = LOW

The NAND Gate

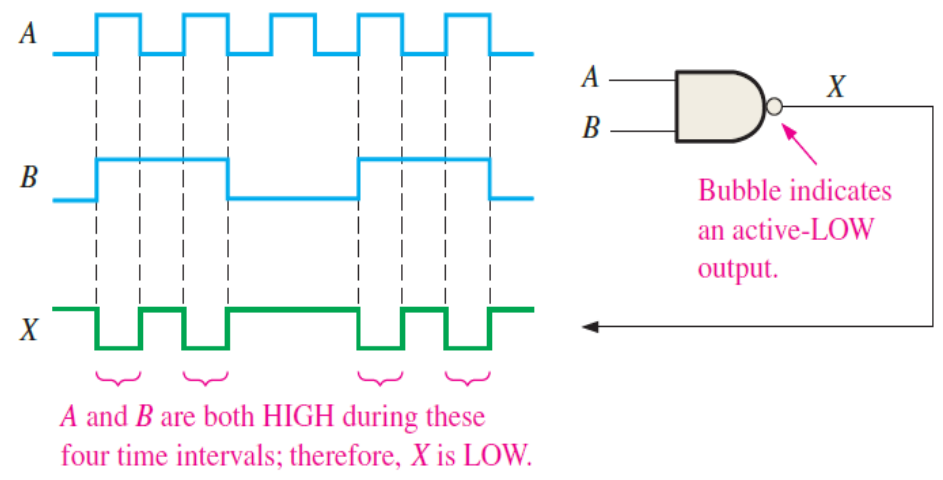
- The NAND gate is a popular logic element because it can be used as a universal gate; that is, NAND gates can be used in combination to perform the AND, OR, and inverter operations.



Inputs		Output
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

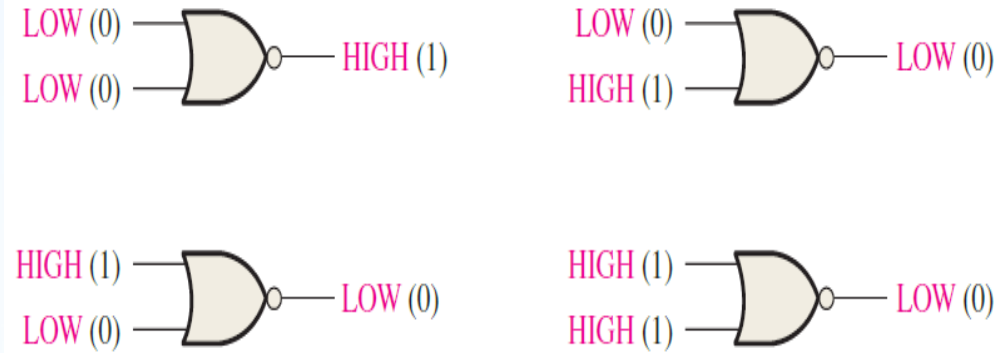
1 = HIGH, 0 = LOW.

- The term *NAND* is a contraction of NOT-AND and implies an AND function with a complemented (inverted) output.



The NOR Gate

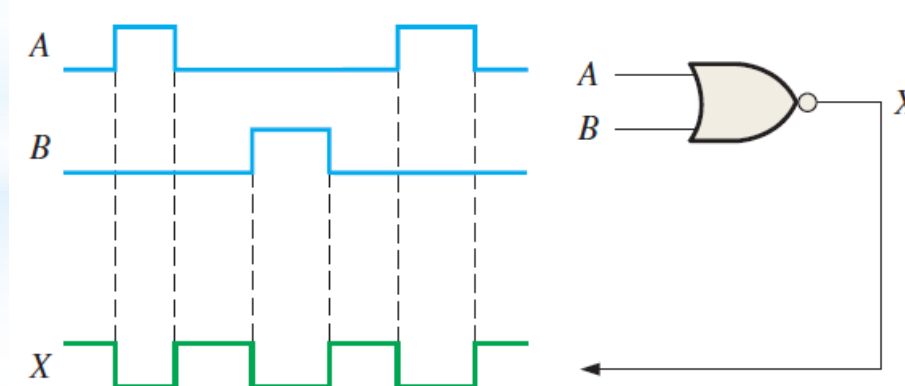
- * The NOR gate, like the NAND gate, is a useful logic element because it can also be used as a universal gate; that is, NOR gates can be used in combination to perform the AND, OR, and inverter operations.



Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

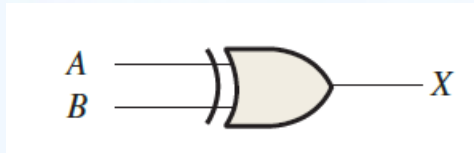
1 = HIGH, 0 = LOW.

- * The term NOR is a contraction of NOT-OR and implies an OR function with an inverted (complemented) output.



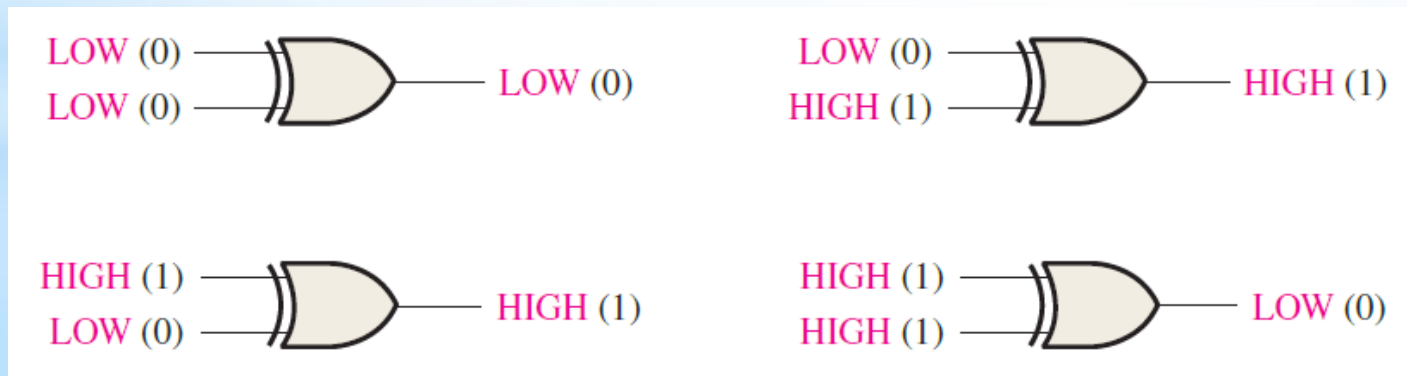
The Exclusive-OR Gate

- * The exclusive-OR gate performs modulo-2 addition. Standard symbols for an exclusive-OR (XOR for short) gate and The Boolean expression for the output of a 2-input XOR gate can be written as:



$$X = \bar{A}B + A\bar{B} = A \oplus B$$

- * The XOR gate has only two inputs. The four possible input combinations and the resulting outputs for an XOR gate. The operation of an XOR gate is summarized in the truth table shown in Table below.



Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

The Exclusive-NOR Gate

- * The bubble on the output of the XNOR symbol indicates that its output is opposite that of the XOR gate. Standard symbols for an exclusive-NOR (XNOR) gate and The Boolean expression for the output of a 2-input XNOR gate can be written as:


$$X = \overline{A} \overline{B} + AB = \overline{A + B}$$

LOW (0) ————
LOW (0) ————



HIGH (1)

LOW (0) ————
HIGH (1) ————



LOW (0)

HIGH (1) ————
LOW (0) ————



LOW (0)

HIGH (1) ————
HIGH (1) ————



HIGH (1)

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

